

MODEL NAME : *VAR00*
PCB NO : *LA-9201P*
BOM P/N : *4619K031L01*
4619K031L02

Dell/Compal Confidential

Mariner 14

Schematic Document

DISCRETE VGA N14P-GT and N14E-GE (optimus)

2012-06-06

Rev: 0.1

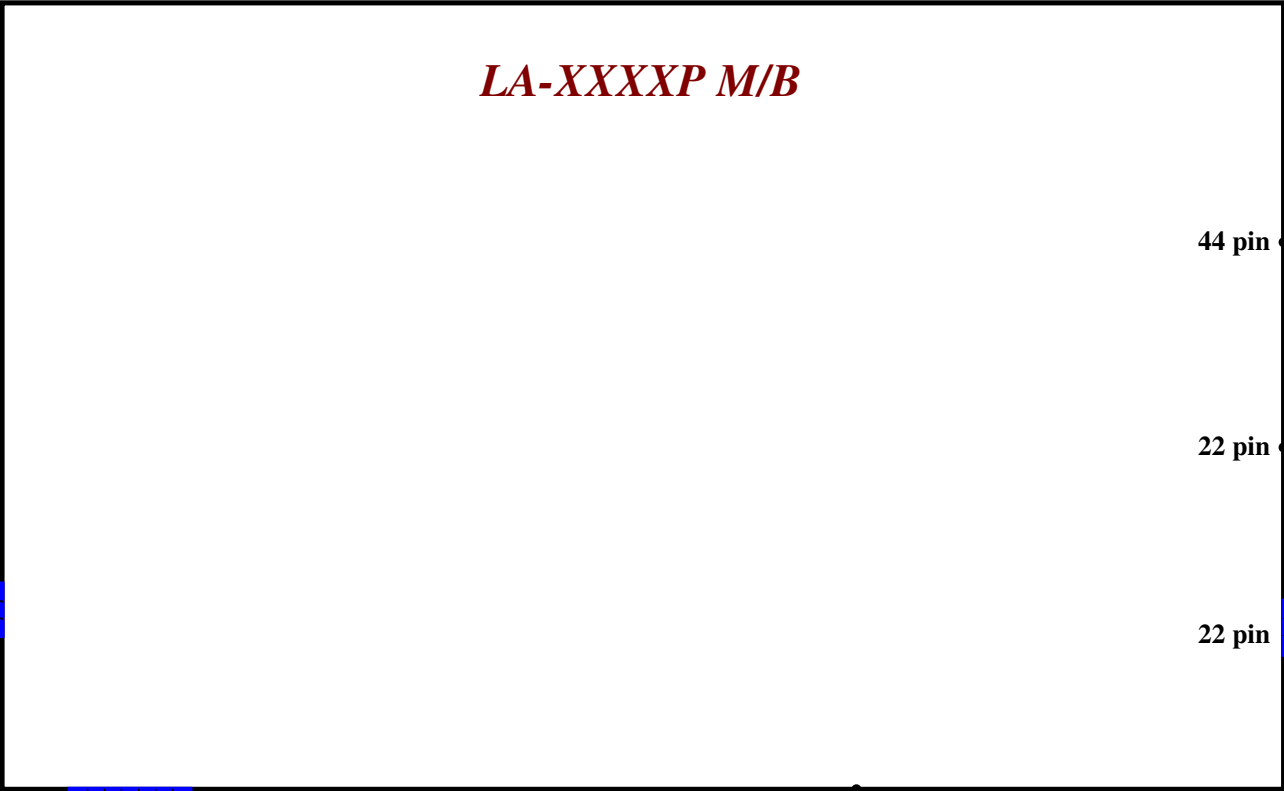
Highlight the short pad for 0 ohm

CONN@ Connector Component
up@ Upsell
en@ Entry
X76@ VARM(SAMSUNG, Hynix)
N14P@ N14P-GT
N14E@ N14E-GE

| | | | | | |
|---|--------------------|-----------------|------------|-------------------------------|---------------|
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| Issued Date | 2011/06/02 | Deciphered Date | 2012/06/02 | Title | |
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| | | | | Document Number | Rev |
| | | | | LA-9201P | 0.1 |
| | | | | Date: Friday, August 10, 2012 | Sheet 1 of 66 |

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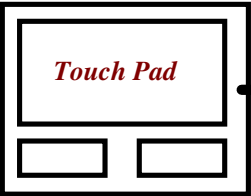
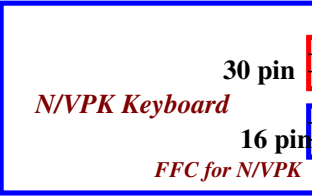
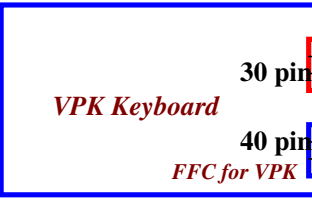
Project Code : VAR00
File Name : LA-9201P



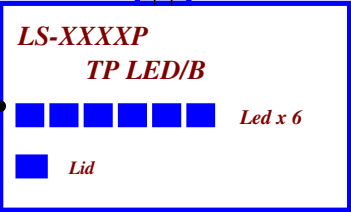
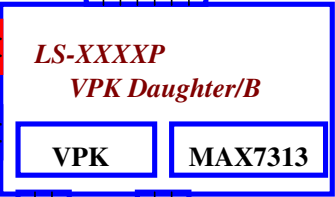
LF-XXXXP
FPC

HDD in ODD Bay Cable

VPK or N/VPK



KSI/KSO



Wire
12pin



| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|---------------|
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| Issued Date | 2011/06/02 | Deciphered Date | 2012/06/02 | Title | Block Diagram |
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| Date: Friday, August 10, 2012 | | Sheet 3 of 66 | | | |

Board ID Table for AD channel

| | | | | | |
|----------|-------------|-------------|-------------|-------------|-----------|
| Vcc | 3.3V +/- 5% | | | | |
| Ra | 100K +/- 5% | | | | |
| Board ID | Rb | VAD_BID min | VAD_BID typ | VAD_BID max | EC AD3 |
| 0 | 0 | 0 V | 0 V | 0.155 V | 0x00-0x0C |
| 1 | 8.2K +/- 5% | 0.168 V | 0.250 V | 0.362 V | 0x0D-0x1C |
| 2 | 18K +/- 5% | 0.375 V | 0.503 V | 0.621 V | 0x1D-0x30 |
| 3 | 33K +/- 5% | 0.634 V | 0.819 V | 0.945 V | 0x31-0x49 |
| 4 | 56K +/- 5% | 0.958 V | 1.185 V | 1.359 V | 0x4A-0x69 |
| 5 | 100K +/- 5% | 1.372 V | 1.650 V | 1.838 V | 0x6A-0x8E |
| 6 | 200K +/- 5% | 1.851 V | 2.200 V | 2.420 V | 0x8F-0xBB |
| 7 | NC | 2.433 V | 3.300 V | 3.300 V | 0xBC-0xFF |

BOARD ID Table

| | |
|----------|--------------|
| Board ID | PCB Revision |
| 0 | 0.1 (SSI) |
| 1 | 0.2 (PT) |
| 2 | 0.3 (ST) |
| 3 | 0.4 (QT) |
| 4 | 1.0 (MP) |
| 5 | |
| 6 | |
| 7 | |

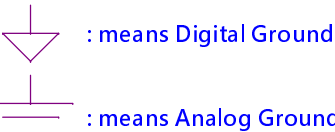
POWER STATES

| Signal | SLP S3# | SLP S4# | SLP S5# | S4 STATE# | SLP M# | ALWAYS PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|---------|---------|---------|-----------|--------|--------------|-----------|-----------|--------|
| State | | | | | | | | | |
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | | HIGH | LOW | ON | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | LOW | ON | OFF | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

PM TABLE

| power plane | +5VALW +3VALW +3VLP +3V_PCH | +1.5V | +5VS +3VS +1.8VS +1.5VS +0.75VS +3VMXM +5VMXM +VCCP +VCCSA +VCC_CORE +1.5V_CPU_VDDQ |
|----------------------|--------------------------------------|-------|---|
| State | | | |
| S0 | ON | ON | ON |
| S3 | ON | ON | OFF |
| S5 S4/AC | ON | OFF | OFF |
| S5 S4/AC don't exist | OFF | OFF | OFF |

Symbol Note :



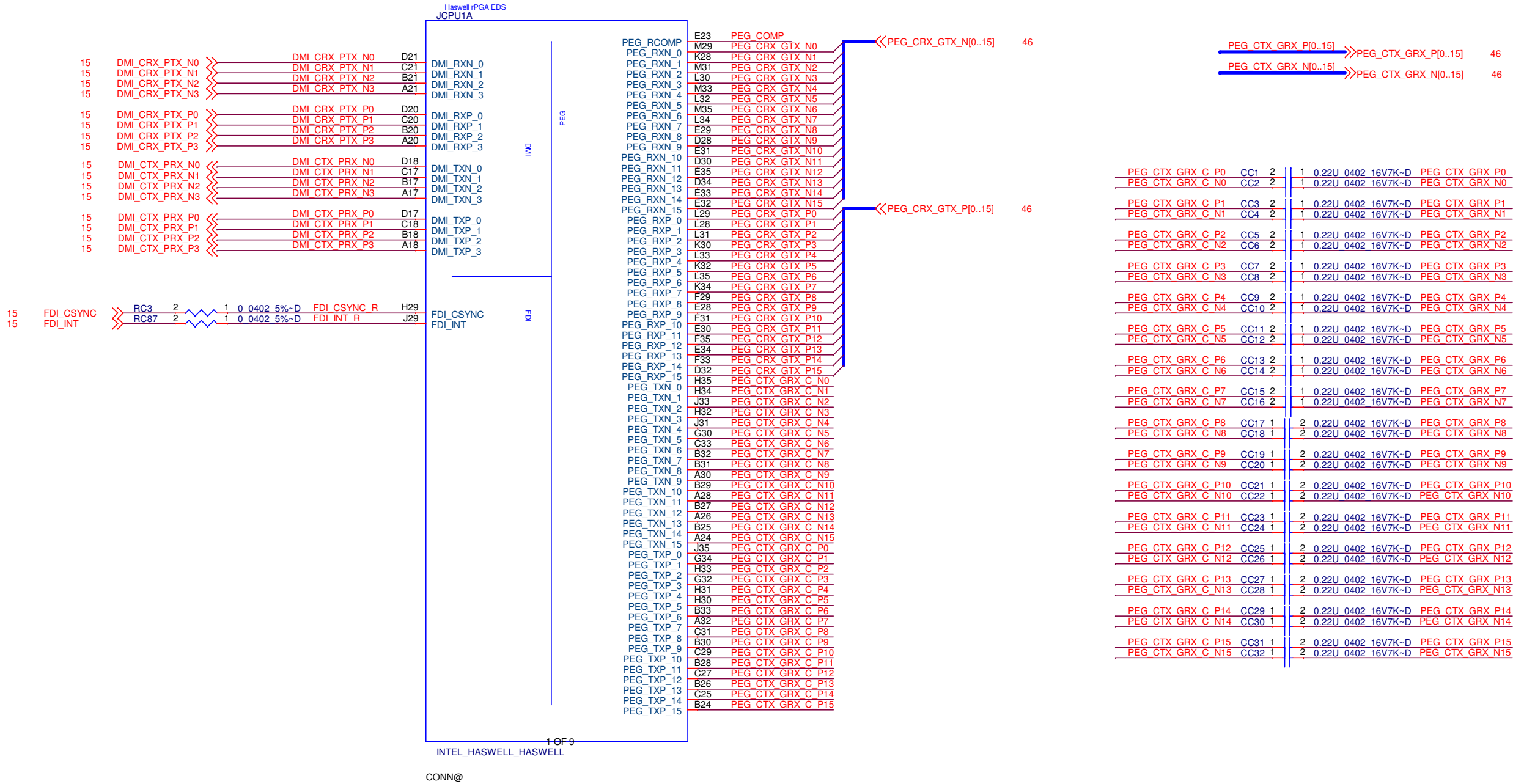
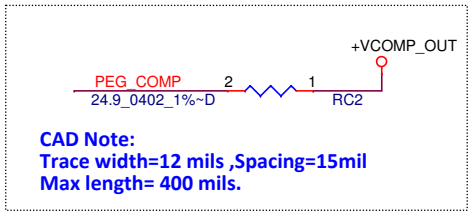
| USB PORT# | DESTINATION |
|-----------|------------------|
| 0 | JUSB1(USB3.0 P1) |
| 1 | JUSB2(USB3.0 P2) |
| 2 | JUSB3(USB3.0 P3) |
| 3 | JUSB4(USB3.0 P4) |
| 4 | JMINI1 (WLAN) |
| 5 | JMINI2 (DMC) |
| 6 | AlienFX/ELC |
| 7 | IR SENSOR |
| 8 | Bluetooth |
| 9 | JESATA |
| 10 | None |
| 11 | eDP CAMERA |
| 12 | LVDS CAMERA |
| 13 | VPK K/B |

| DIFFERENTIAL | DESTINATION | FLEX CLOCKS | DESTINATION |
|--------------|------------------|-------------|-------------|
| CLKOUT_PCIE0 | MINI CARD-1 WLAN | CLKOUTFLEX0 | None |
| CLKOUT_PCIE1 | MINI CARD-2 DMC | CLKOUTFLEX1 | None |
| CLKOUT_PCIE2 | 10/100/1G LAN | CLKOUTFLEX2 | None |
| CLKOUT_PCIE3 | CARD READER | CLKOUTFLEX3 | None |
| CLKOUT_PCIE4 | None | | |
| CLKOUT_PCIE5 | None | | |
| CLKOUT_PCIE6 | None | | |
| CLKOUT_PCIE7 | None | | |
| CLKOUT_PEG_A | NV | | |

| CLKOUT | DESTINATION |
|--------|-------------------|
| PCI0 | PCH_LOOPBACK |
| PCI1 | EC |
| PCI2 | 80port debug card |
| PCI3 | None |
| PCI4 | None |

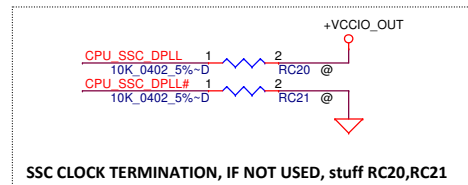
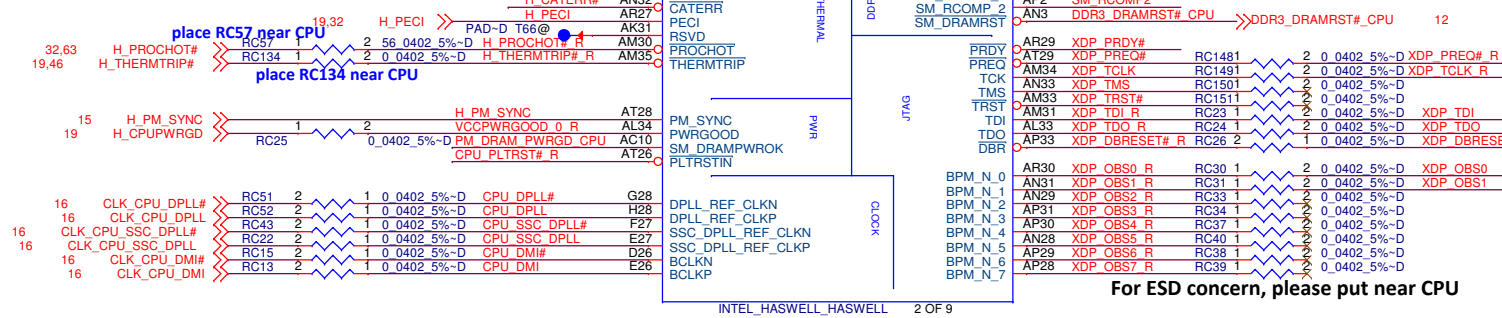
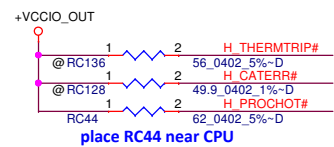
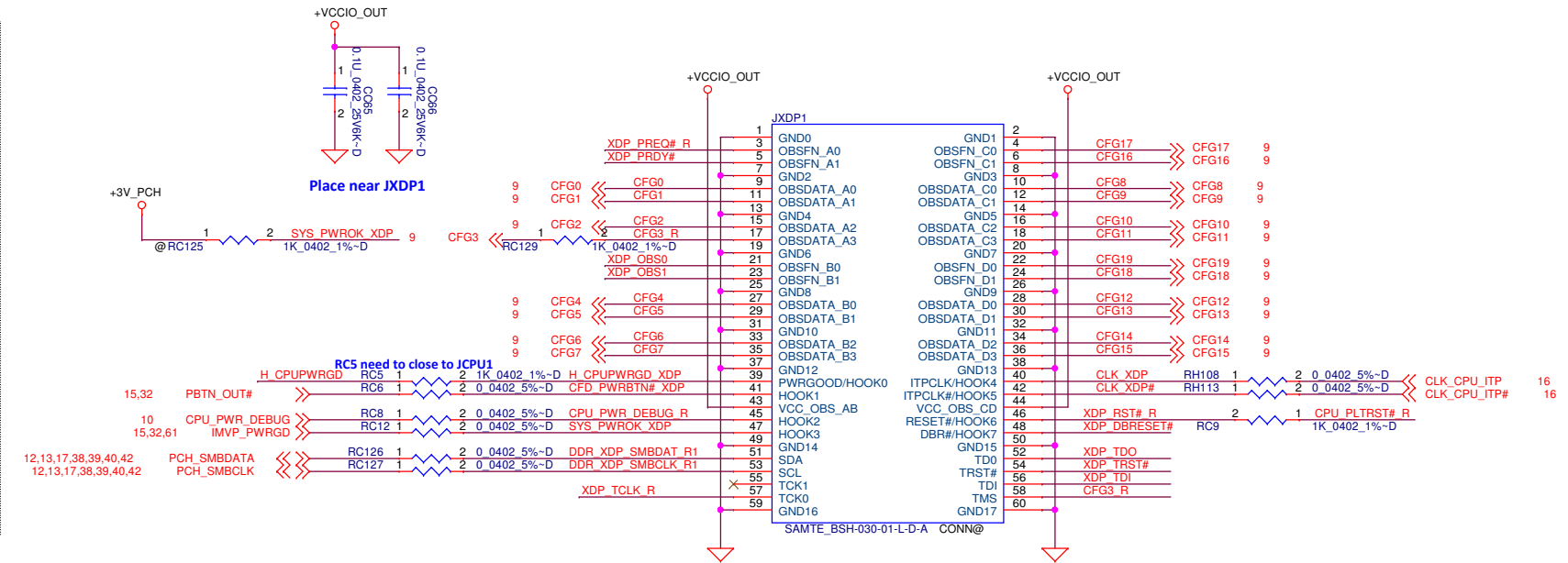
| SATA III | DESTINATION |
|----------|------------------|
| SATA0 | HDD1 |
| SATA1 | None |
| SATA2 | ODD |
| SATA3 | mSATA |
| SATA4 | MINI CARD-1 WLAN |
| SATA5 | MINI CARD-2 MDC |

| PCI EXPRESS | DESTINATION |
|-------------|---------------|
| Lane 1 | None |
| Lane 2 | None |
| Lane 3 | 10/100/1G LAN |
| Lane 4 | CARD READER |
| Lane 5 | None |
| Lane 6 | None |
| Lane 7 | None |
| Lane 8 | None |



15_SM_DRAMPWROK with DDR Power Gating Topology

The schematic diagram illustrates the 15_SM_DRAMPWROK circuit with DDR Power Gating Topology. The circuit includes a 74AHC1G09GW_TSSOP-5 (UC2) inverter, a 3.3K resistor (RC14), a 100K resistor (RC89), a 100nF capacitor (CC156), and a 0.1uF capacitor (C156). It also features a 3.3K resistor (RC28) and a 100nF capacitor (CC156). The circuit is powered by +3V_PCH and +1.35V_CPU_VDDQ. Signals include SYS_PWROK, PM_DRAM_PWRGD, RUNPWROK AND, and RUN_ON_CPU1.5VS3#.



Buffered reset to CPU

UC1: SN74LVC1G07DCKR_SC70-5-D

Inputs: PLT_RST# (X), GND (3)

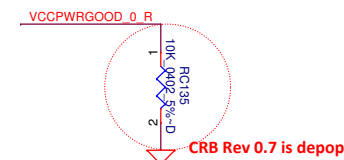
Outputs: PCH_PLTRST# BUF (4), Y (5)

Power: +3VS, +1.05VS

Resistors: RC17 (1K 0402 1%-D), RC10 (43_0402_5%-D), RC11 (2K 0402 5%-D)

Capacitor: CC140 (0.1u 0402 25V6K-D)

CAD Note: PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU



CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130

SM RCOMP0 RC45 1 2 100 0402 1%~D
SM RCOMP1 RC55 1 2 75 0402 1%~D
SM RCOMP2 RC49 1 2 100 0402 1%~D

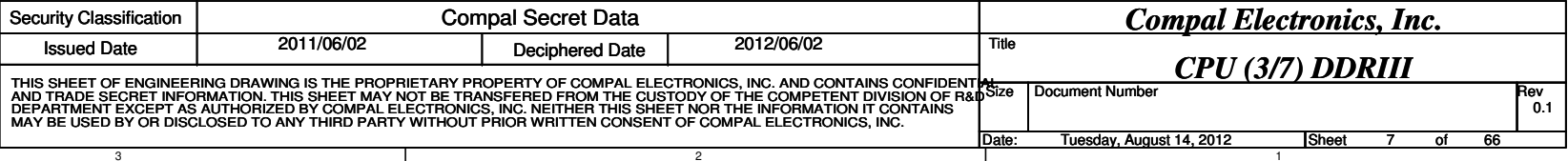
CAD Note:
 Trace width=12~15 mil, Spcing=20 mils
 Max trace length= 500 mil

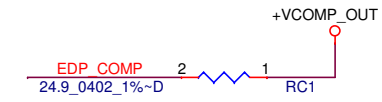
The diagram shows the timing of the RC192 module signals. The signals are:

- XDP_DBRESET#**: Active low reset signal, connected to RC19 2.
- XDP_TMS**: Test Mode Select signal, connected to @RC27 2.
- XDP_TDI_R**: Test Data In/Receive signal, connected to RC29 2.
- XDP_PREQ#**: Precharge Enable signal, connected to @RC32 2.
- XDP_TDO_R**: Test Data Out/Receive signal, connected to RC35 2.
- XDP_TCLK**: Test Clock signal, connected to RC42 2.
- XDP_TRST#**: Active low reset signal, connected to RC41 2.

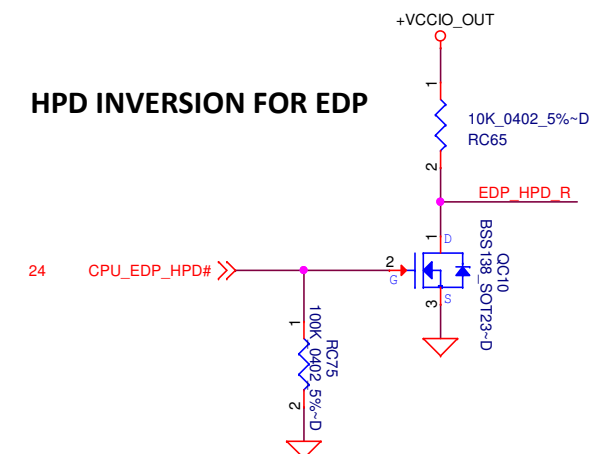
The timing parameters for all signals are: 1 51 0402 1%-D. The diagram also shows a +3VS supply voltage and a +1.05VS supply voltage.

| | | | | | |
|---|------------|--------------------|------------|--------------------------|----------------------|
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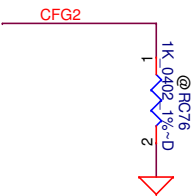


**CAD Note:Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.**

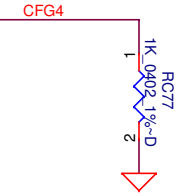


| | | | | | | |
|---|------------|--------------------|------------|---------------------------------|------------------------------|------------|
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| 3 | | 2 | | Date: Tuesday, August 14, 2012 | Sheet 8 of 66 | 1 |

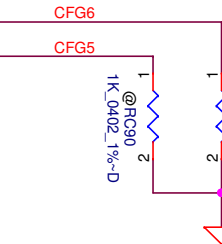
CFG STRAPS for CPU



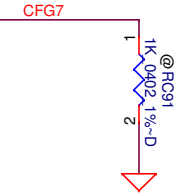
| PEG Static Lane Reversal - CFG2 is for the 16x | |
|--|--|
| CFG2 | 1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed |



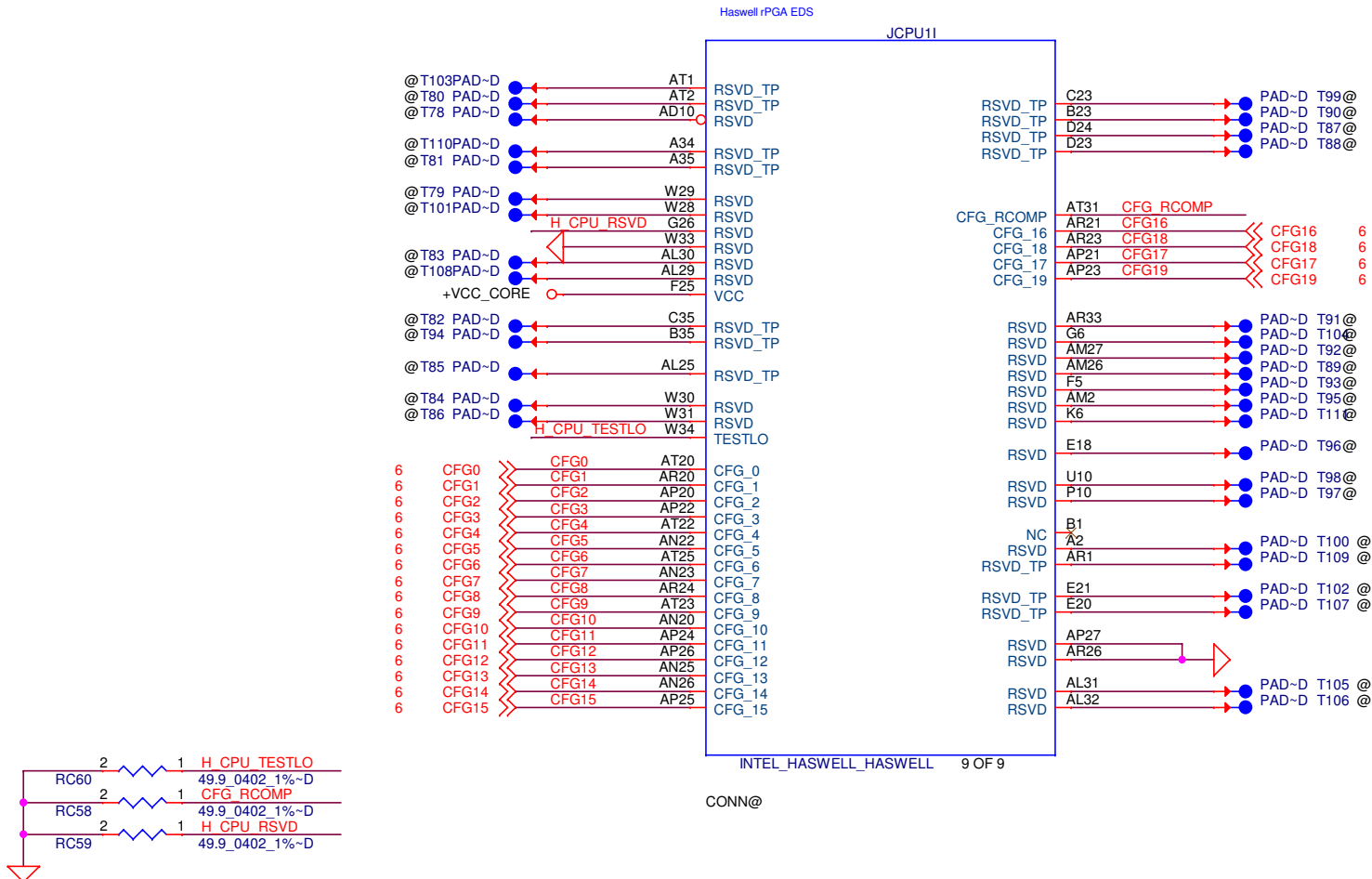
| Display Port Presence Strap | |
|-----------------------------|--|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |



| PCIe Port Bifurcation Straps | |
|------------------------------|--|
| CFG[6:5] | 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |

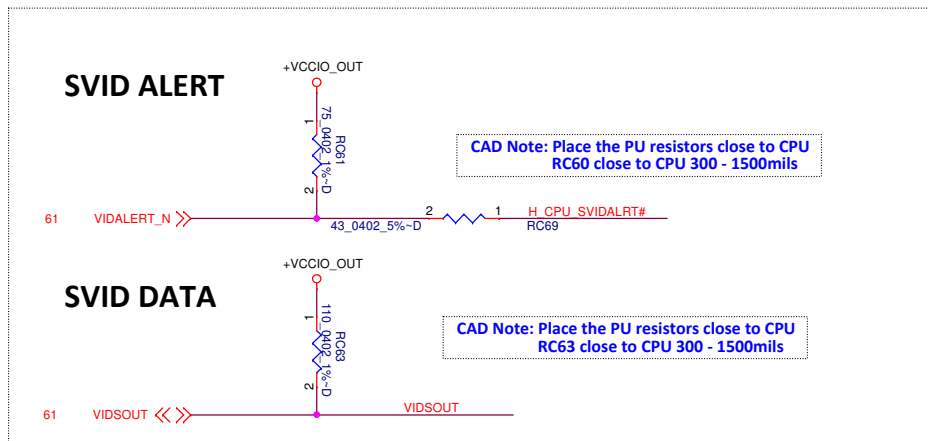
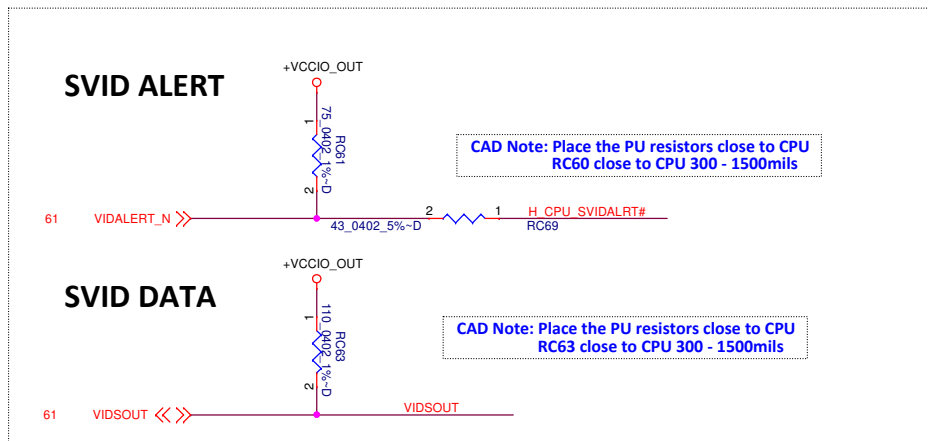


| PEG DEFER TRAINING | |
|--------------------|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training |



+1.35V_CPU_VDDQ Source

The schematic diagram illustrates the +1.35V_CPU_VDDQ source circuit. It features a power supply network starting from a +3VALW input, passing through a resistor network (RC74, RC72) and a MOSFET (OC4A) to a node labeled 'RUN ON CPU1.5VS3#'. This node is connected to a MOSFET (OC4B) and a resistor (RC73) leading to a +1.35V_CPU_VDDQ output. A MOSFET (QC3, AO4304L) is also shown, connected to a +1.35V input and a node labeled 'RUN ON CPU1.5VS3'. Various capacitors (CC135, CC136, CC138) and resistors (RC143, RC144) are used for decoupling and timing. The circuit is labeled with component values and part numbers.



VCC_SENSE

+VCC_CORE

100 nF RC66

0.0402 5% RC67

VCCSENSE

CAD Note: RC67 SHOULD BE PLACED CLOSE TO CPU

VSSSENSE

0.0402 5% RC68

VSSSENSE_R

CAD Note: RC68 SHOULD BE PLACED CLOSE TO CPU

VCC_SENSE

+VCC_CORE

100 nF RC66

0.0402 5% RC67

VCCSENSE

VCCSENSE_R

CAD Note: RC67 SHOULD BE PLACED CLOSE TO CPU

VSSSENSE

VSSSENSE_R

RC68

CAD Note: RC68 SHOULD BE PLACED CLOSE TO CPU

VCC_SENSE

+VCC_CORE

100 nF RC66

0.0402 5% RC67

VCCSENSE

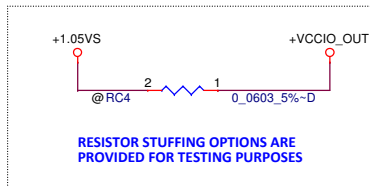
CAD Note: RC67 SHOULD BE PLACED CLOSE TO CPU

VSSSENSE

0.0402 5% RC68

VSSSENSE_R

CAD Note: RC68 SHOULD BE PLACED CLOSE TO CPU



VDDQ DECOUPLING

3300 DZ 2VW, R6M-D

CC167

CC168

CC169

CC170

CC180

CC181

CC182

CC183

CC184

CC185

CC186

CC187

CC188

CC189

CC190

CC191

CC192

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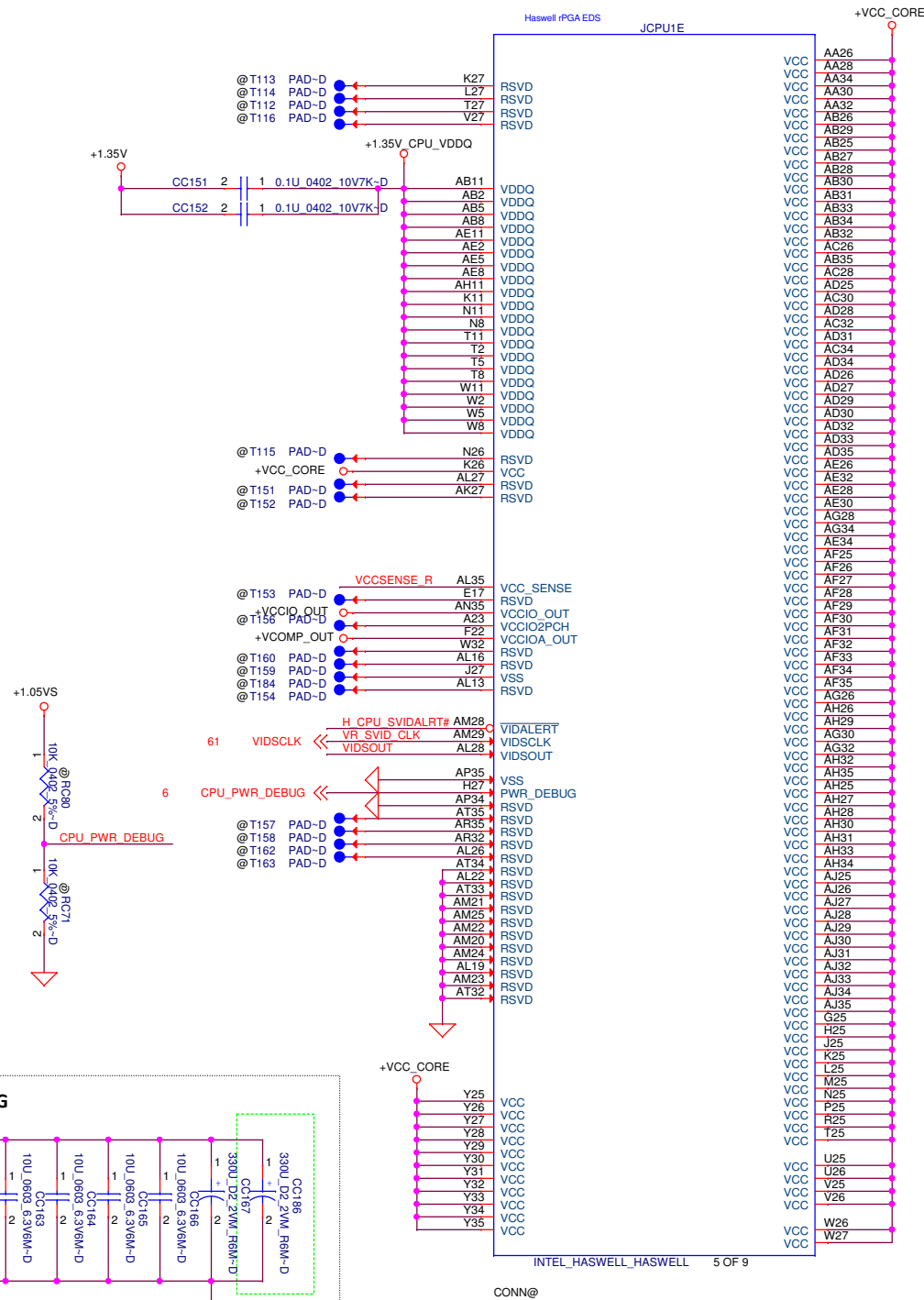
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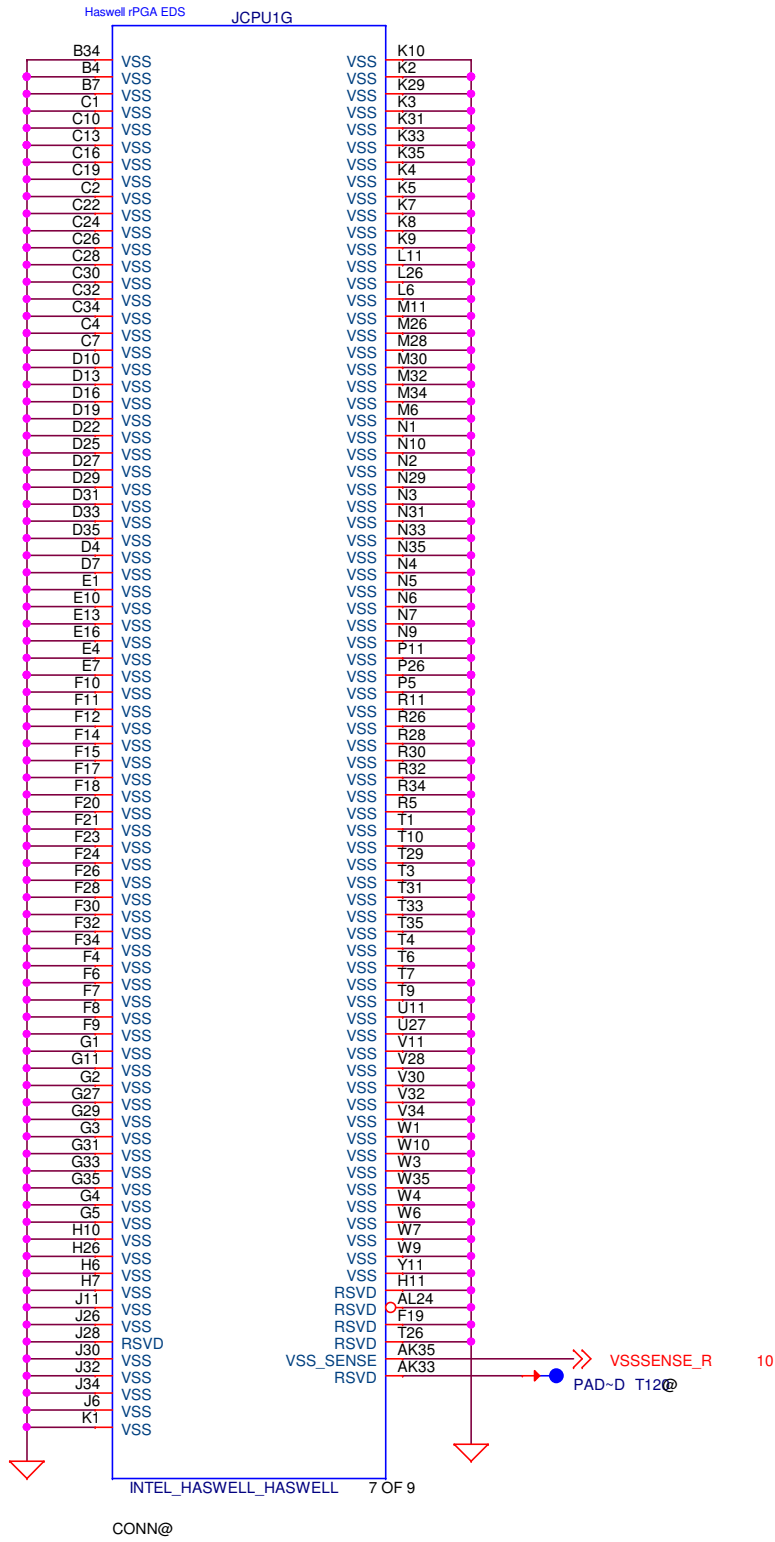
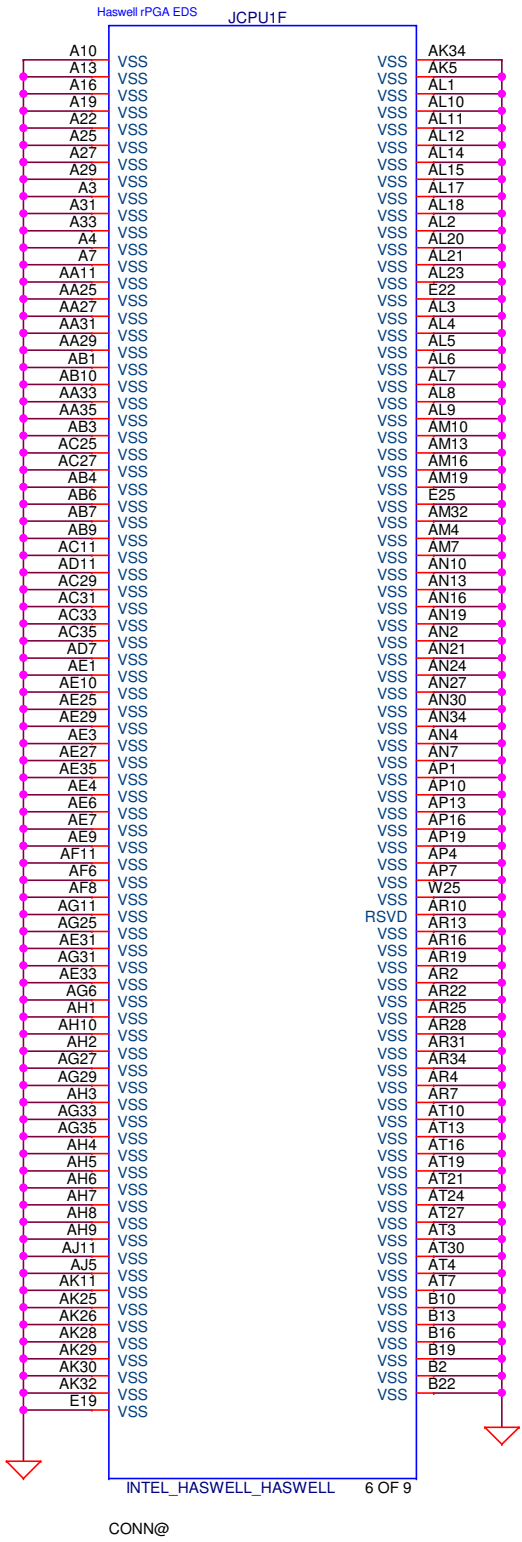
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CC563

CC5



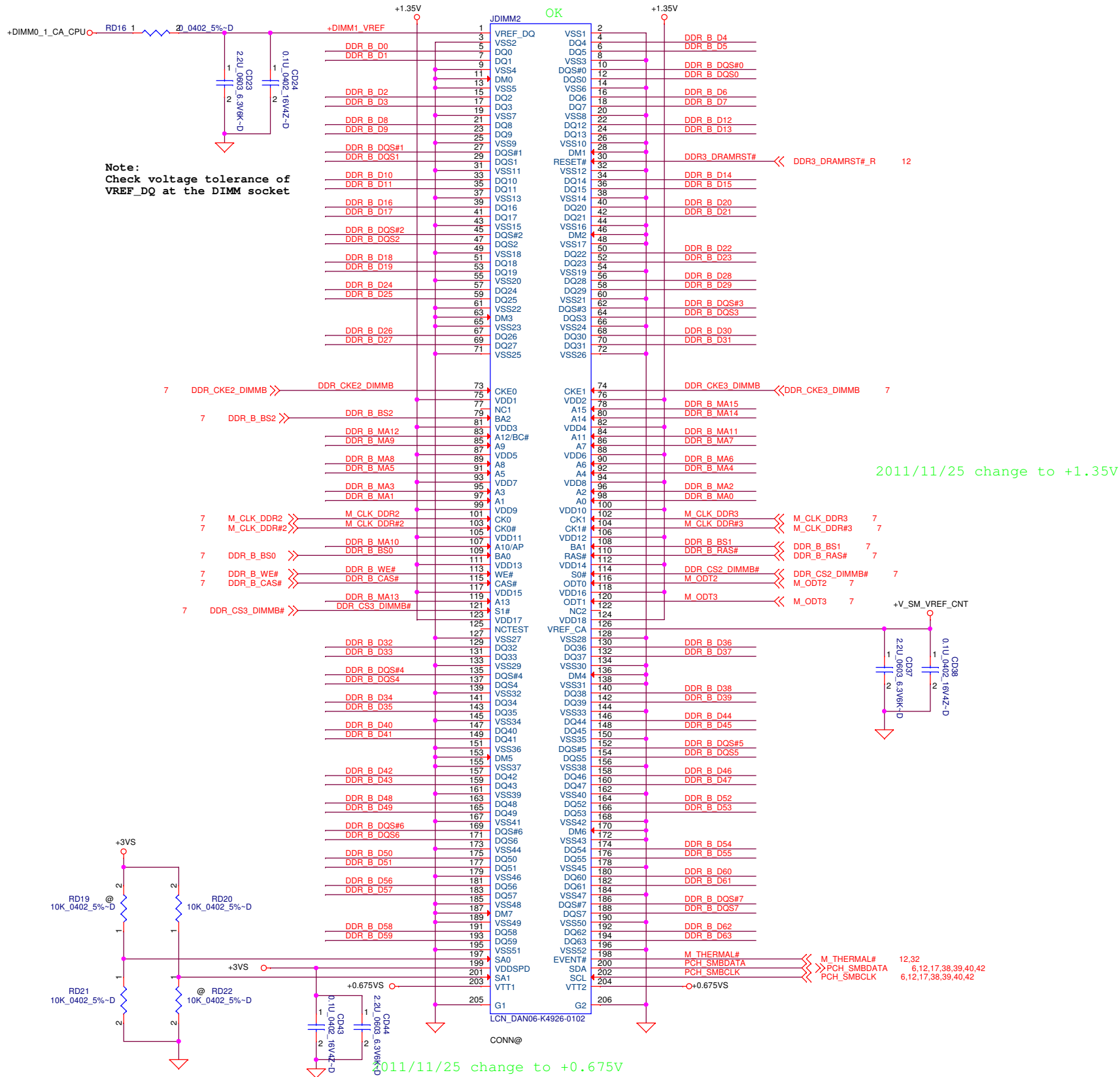
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|---|--------------------------|--------------------|------------|---|-----|
| Security Classification | | Compal Secret Data | | <i>Compal Electronics, Inc.</i> CPU (6/7) PWR | |
| Issued Date | 2012/02/28 | Deciphered Date | 2013/02/27 | Title | |
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| | | | | Customer | 0.1 |
| Date: | Tuesday, August 14, 2012 | Sheet | 10 of 66 | | |

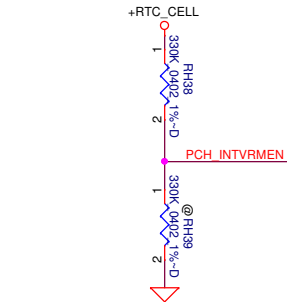


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|---|--------------------|-----------------|------------|--------------------------------|--------------------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2012/02/28 | Deciphered Date | 2013/02/27 | Title | CPU (7/7) VSS |
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| | | | | Date: Tuesday, August 14, 2012 | Rev 0.1 |
| | | | | Sheet 11 of 66 | |

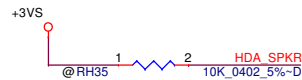
H:9.2

2011/11/25 change to +1.35V

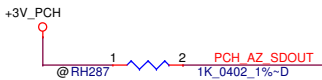




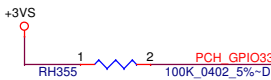
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs



NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH



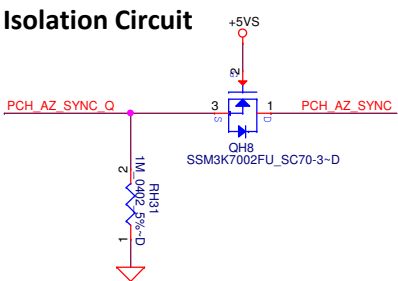
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED



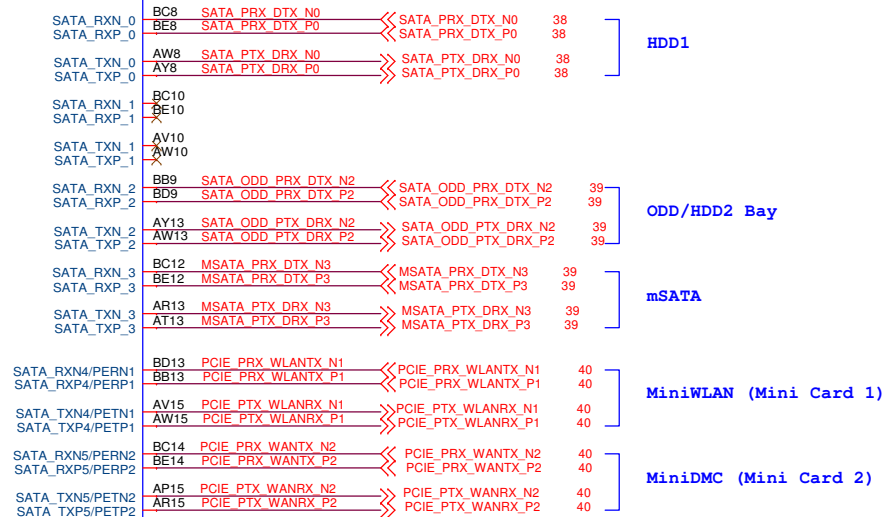
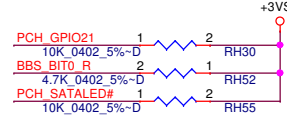
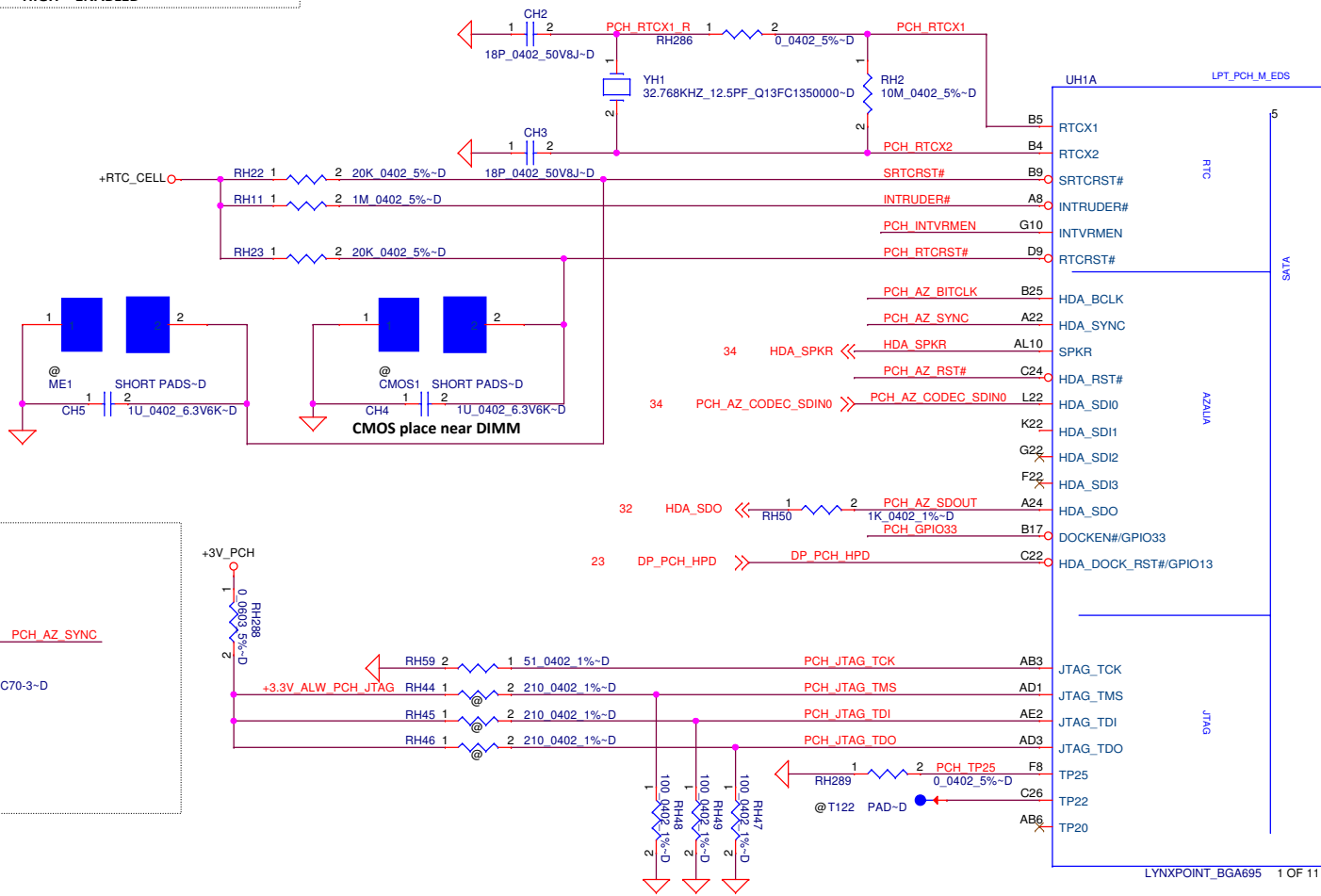
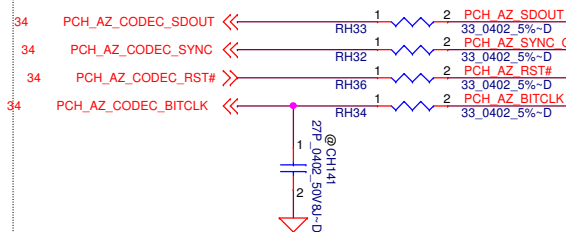
| CMOS_CLR1 | CMOS setting |
|-----------|--------------|
| Shunt | Clear CMOS |
| Open | Keep CMOS |

| ME_CLR1 | TPM setting |
|---------|------------------------|
| Shunt | Clear ME RTC Registers |
| Open | Keep ME RTC Registers |

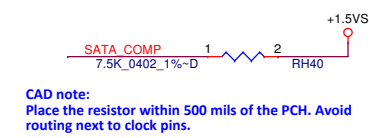
HDA_SYNC Isolation Circuit

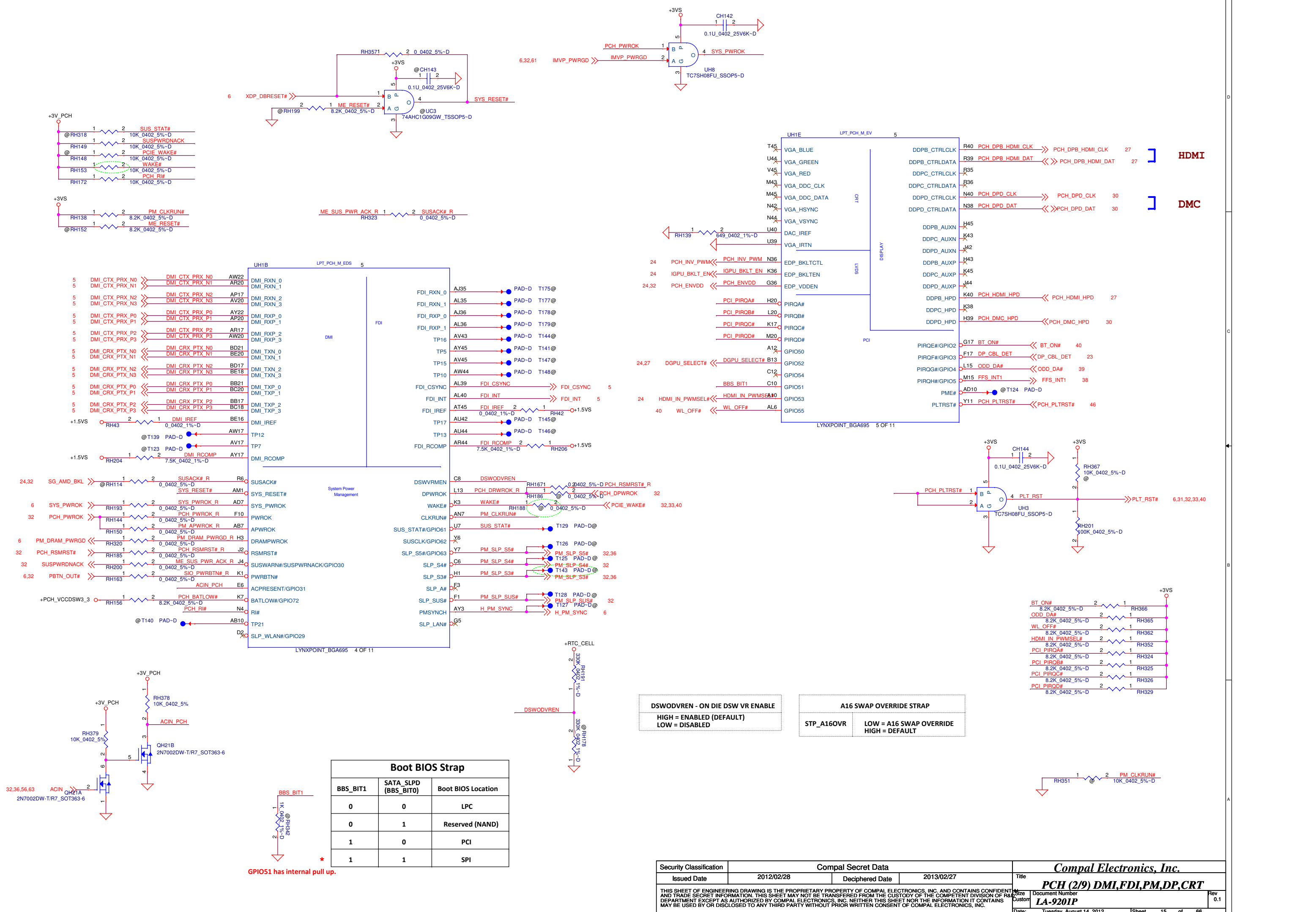


HDA for Codec and MDC



SATA Impedance Compensation





| Boot BIOS Strap | | |
|-----------------|----------------------|--------------------|
| BBS_BIT1 | SATA_SLPD (BBS_BIT0) | Boot BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved (NAND) |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

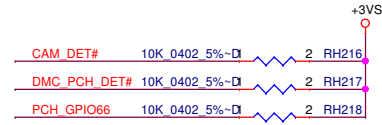
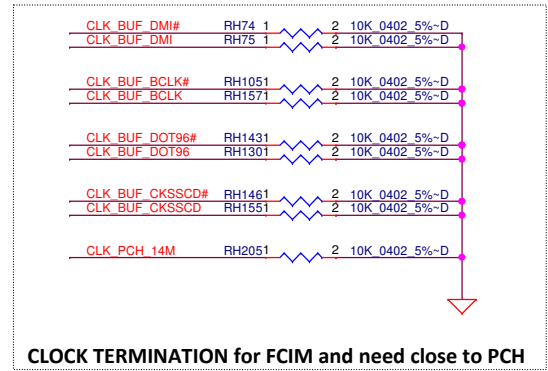
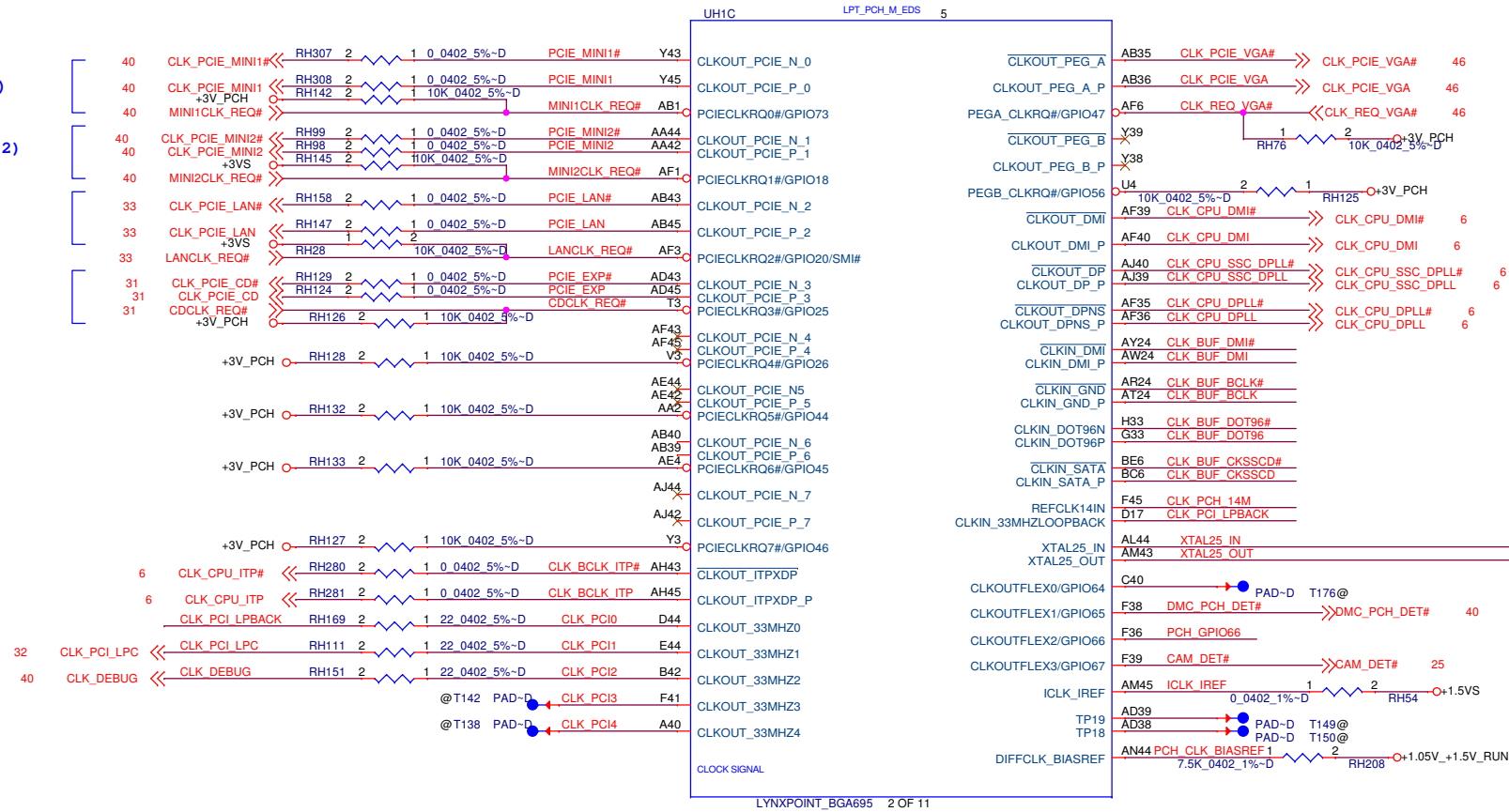
A16 SWAP OVERRIDE STRAP
STP_A16OVR LOW = A16 SWAP OVERRIDE
HIGH = DEFAULT

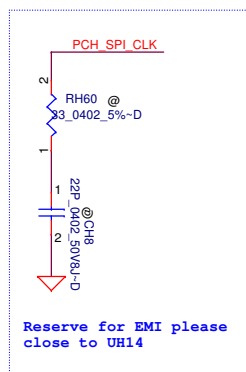
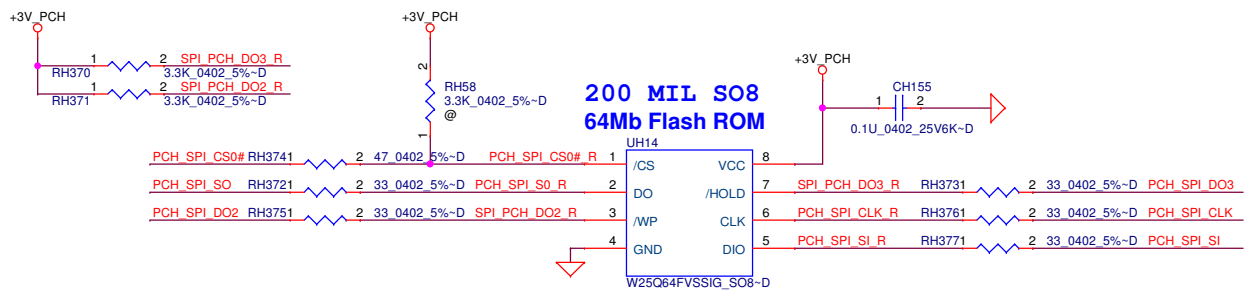
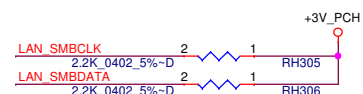
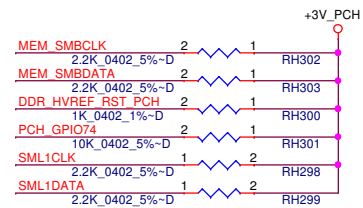
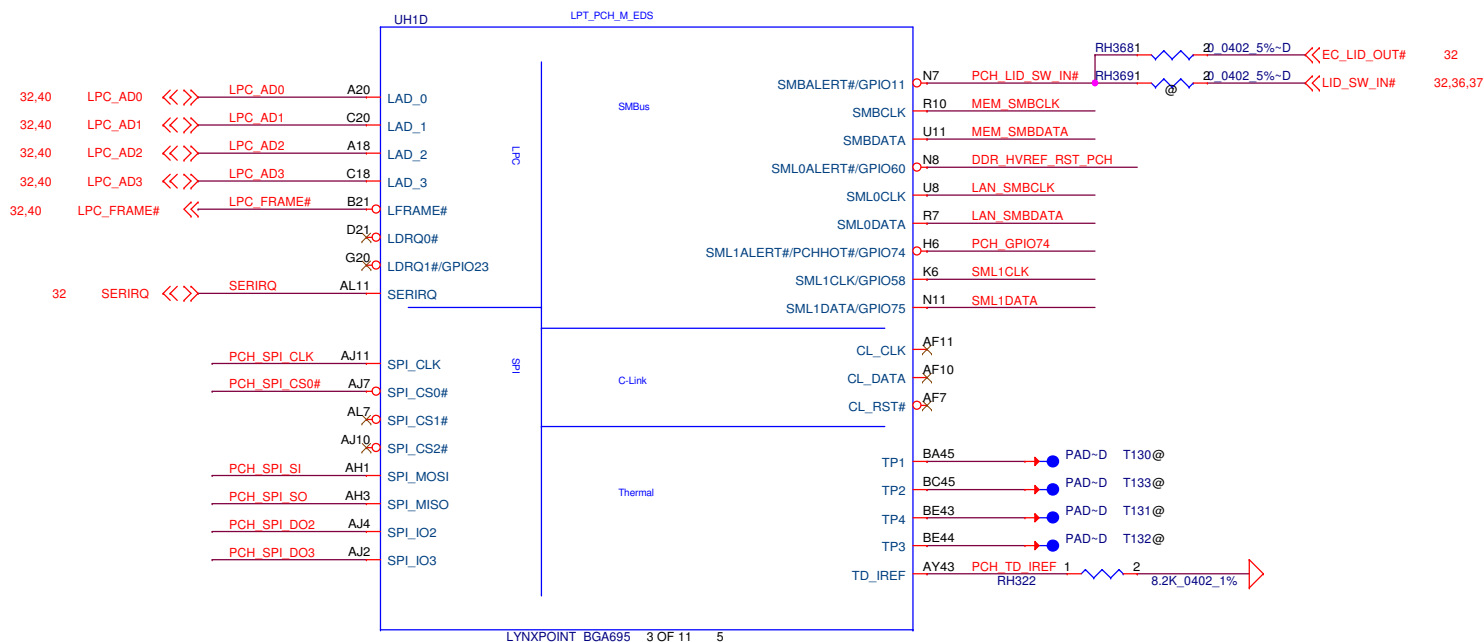
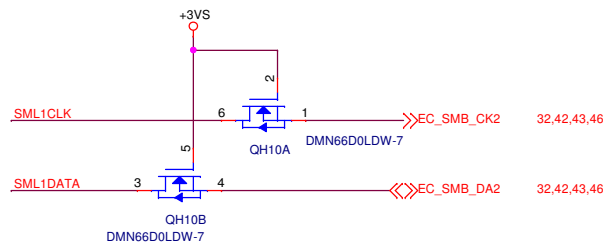
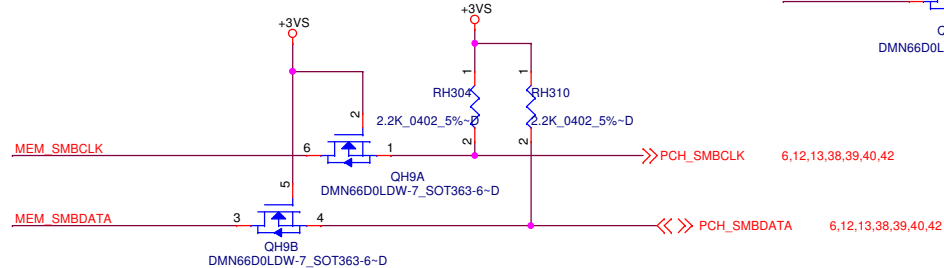
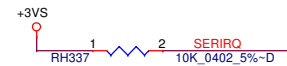
MiniWLAN
(Mini Card 1)

DMC (Mini Card 2)

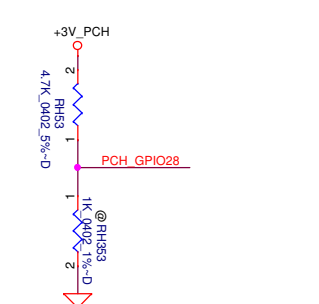
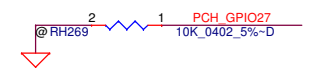
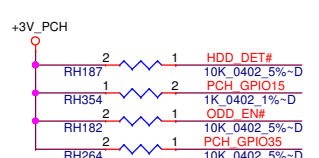
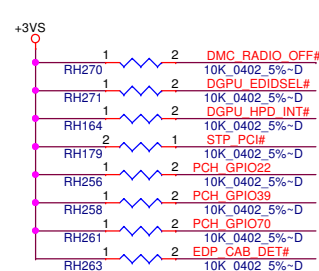
10/100/1G LAN

Card Reader

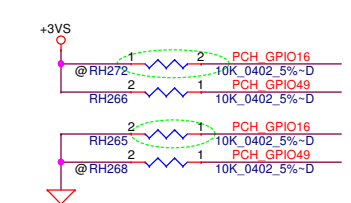




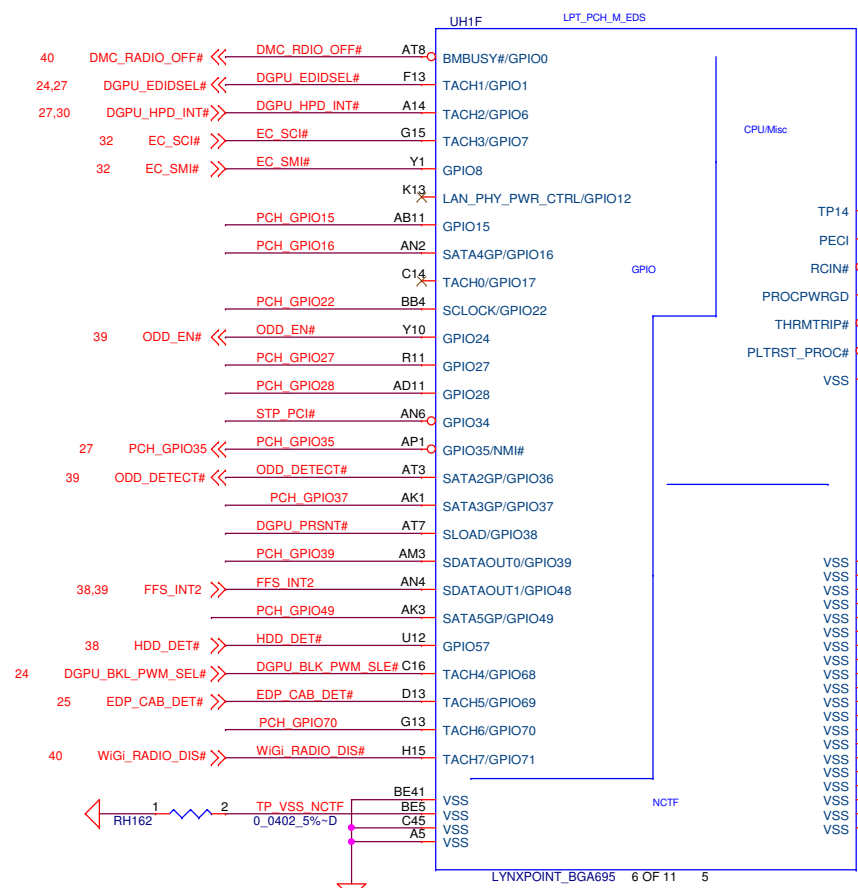
| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|-------------------------|
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| Issued Date | 2012/02/28 | Deciphered Date | 2013/02/27 | Compal Electronics, Inc. | |
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| | | | | LA-9201P | 0.1 |
| | | | | Date: | Monday, August 20, 2012 |
| | | | | Sheet | 17 of 66 |



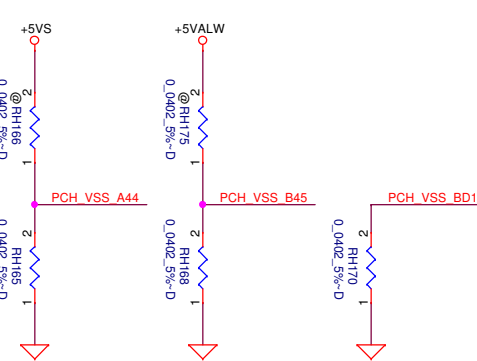
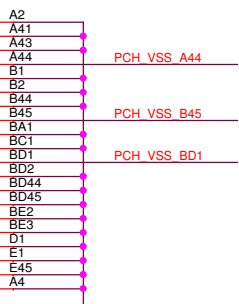
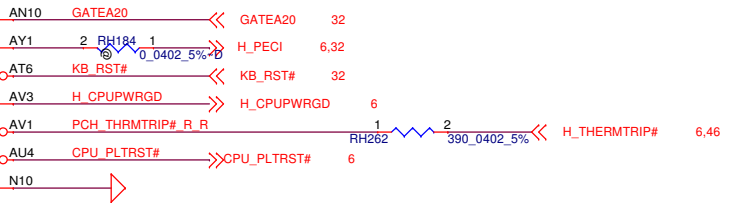
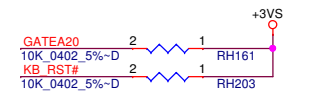
PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW



| Config | GPIO16,49 |
|----------------------|-----------|
| USB X4,PCIEX8,SATAx6 | 11 |
| USB X6,PCIEX8,SATAx4 | 01 |

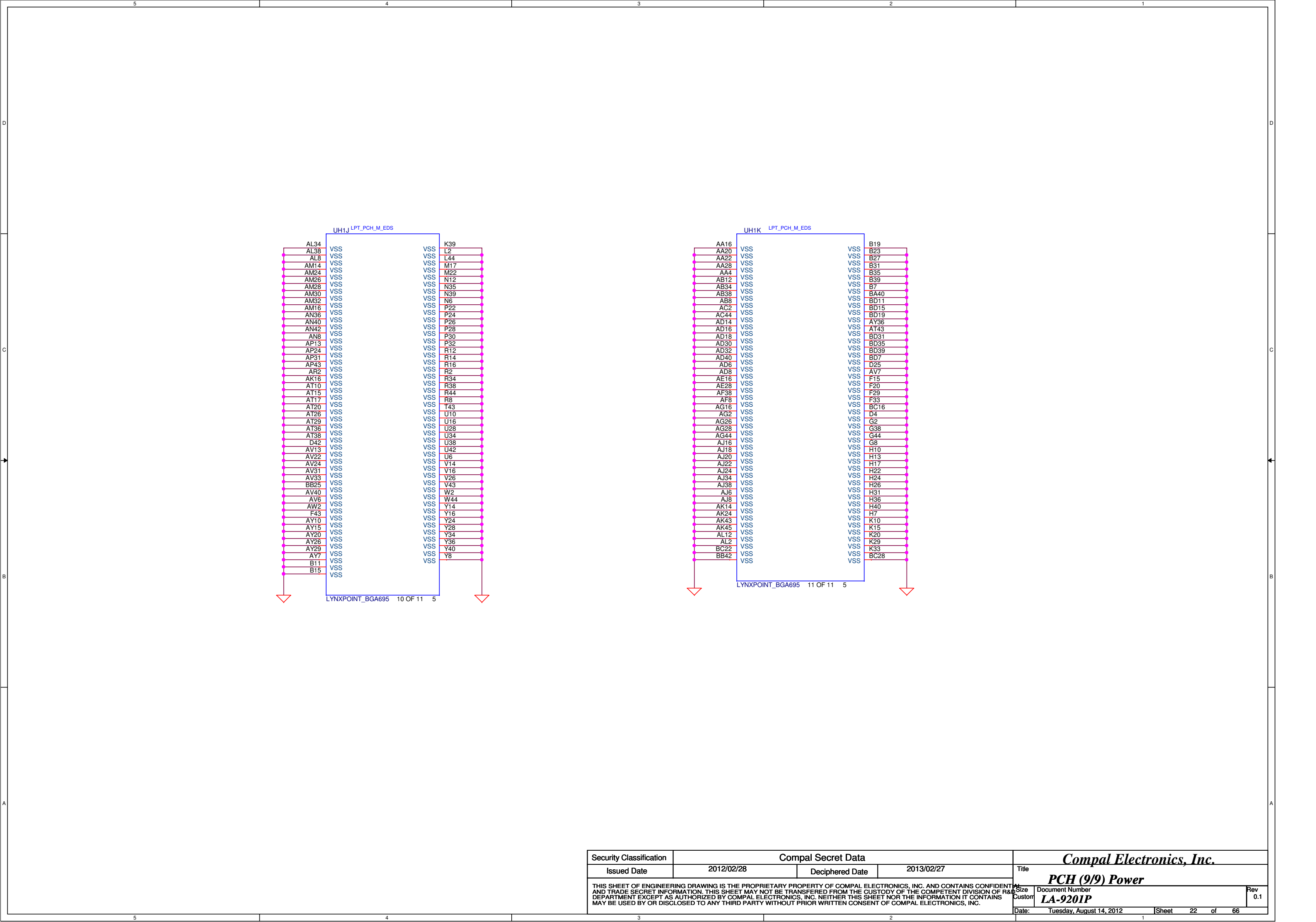


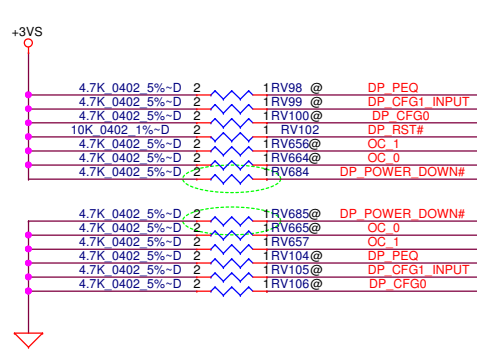
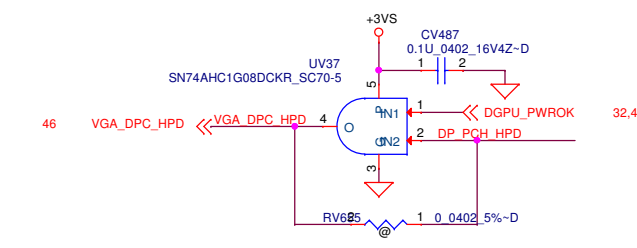
For BIOS setting dGPU present
* LOW - dGPU exist



SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

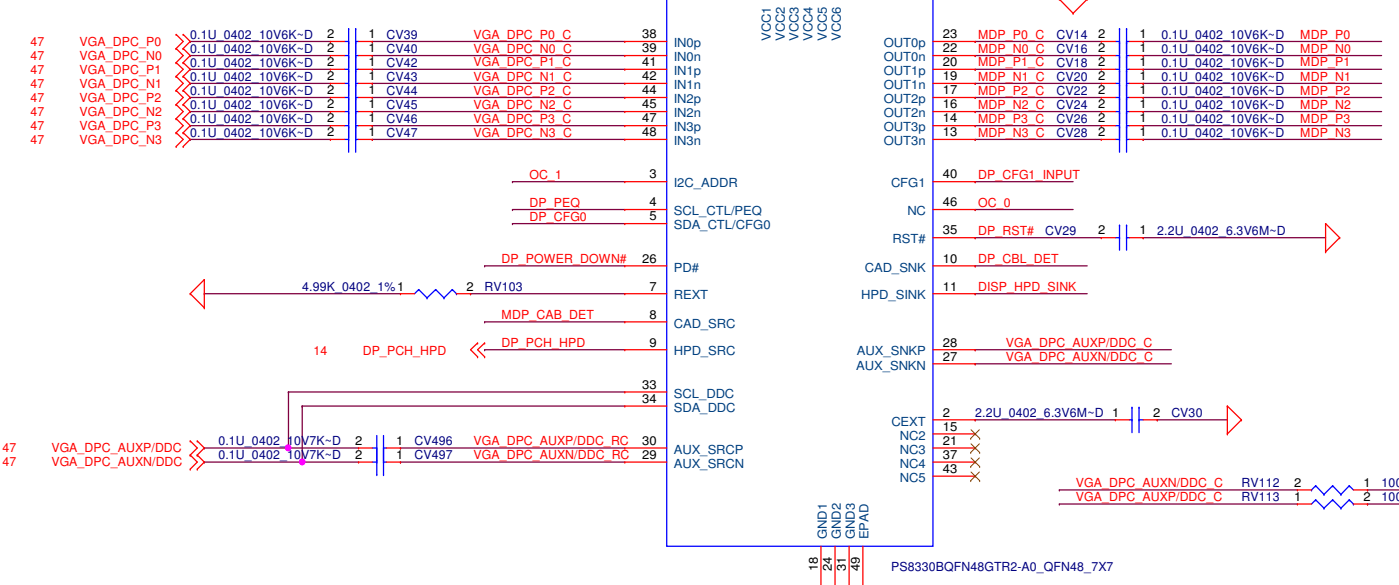
| Fixed Signals | | | | Muxed Signals | | Fixed Signals | | | | | | Muxed Signals | | Fixed Signals | | | |
|---------------|--------|--------|--------|---------------|--------|---------------|--------|--------|--------|--------|--------|---------------|--------|---------------|--------|--------|--------|
| USB3 1 | USB3 2 | USB3 5 | USB3 6 | PCIE 1 | PCIE 2 | PCIE 3 | PCIE 4 | PCIE 5 | PCIE 6 | PCIE 7 | PCIE 8 | SATA 4 | SATA 5 | SATA 0 | SATA 1 | SATA 2 | SATA 3 |
| | | | | (00) | (00) | | | | | | | (00) | (00) | | | | |
| | | | | USB3 3 | USB3 4 | | | | | | | PCIE 1 | PCIE 2 | | | | |
| | | | | (01) | (01) | | | | | | | (01) | (01) | | | | |



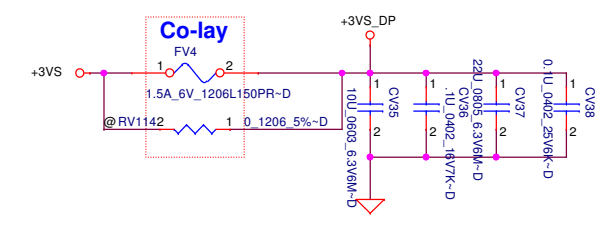


DP Redriver

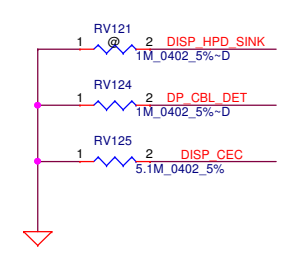
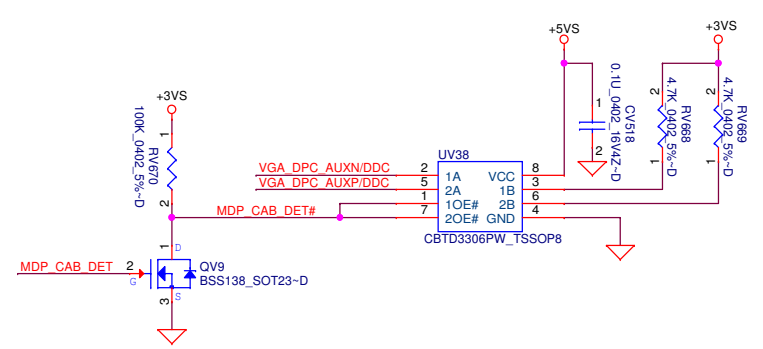
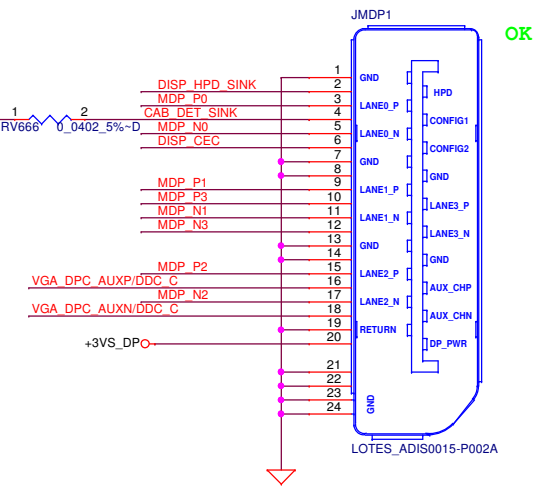
GPU



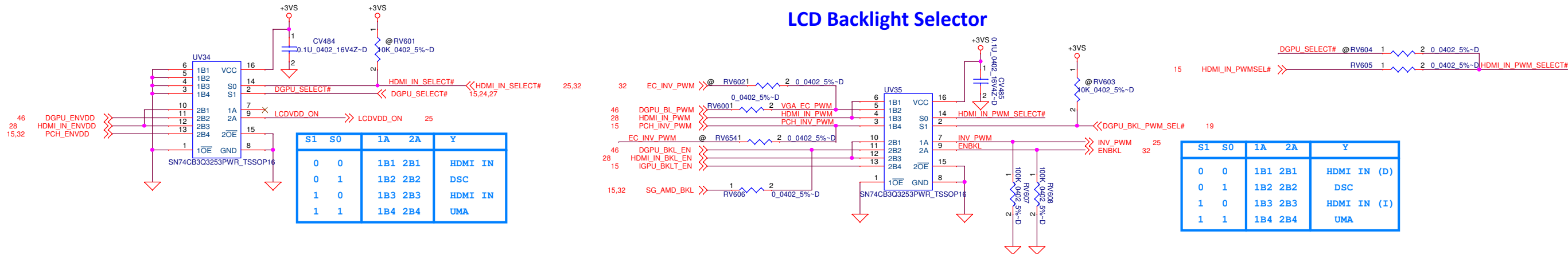
Need apply CIS part



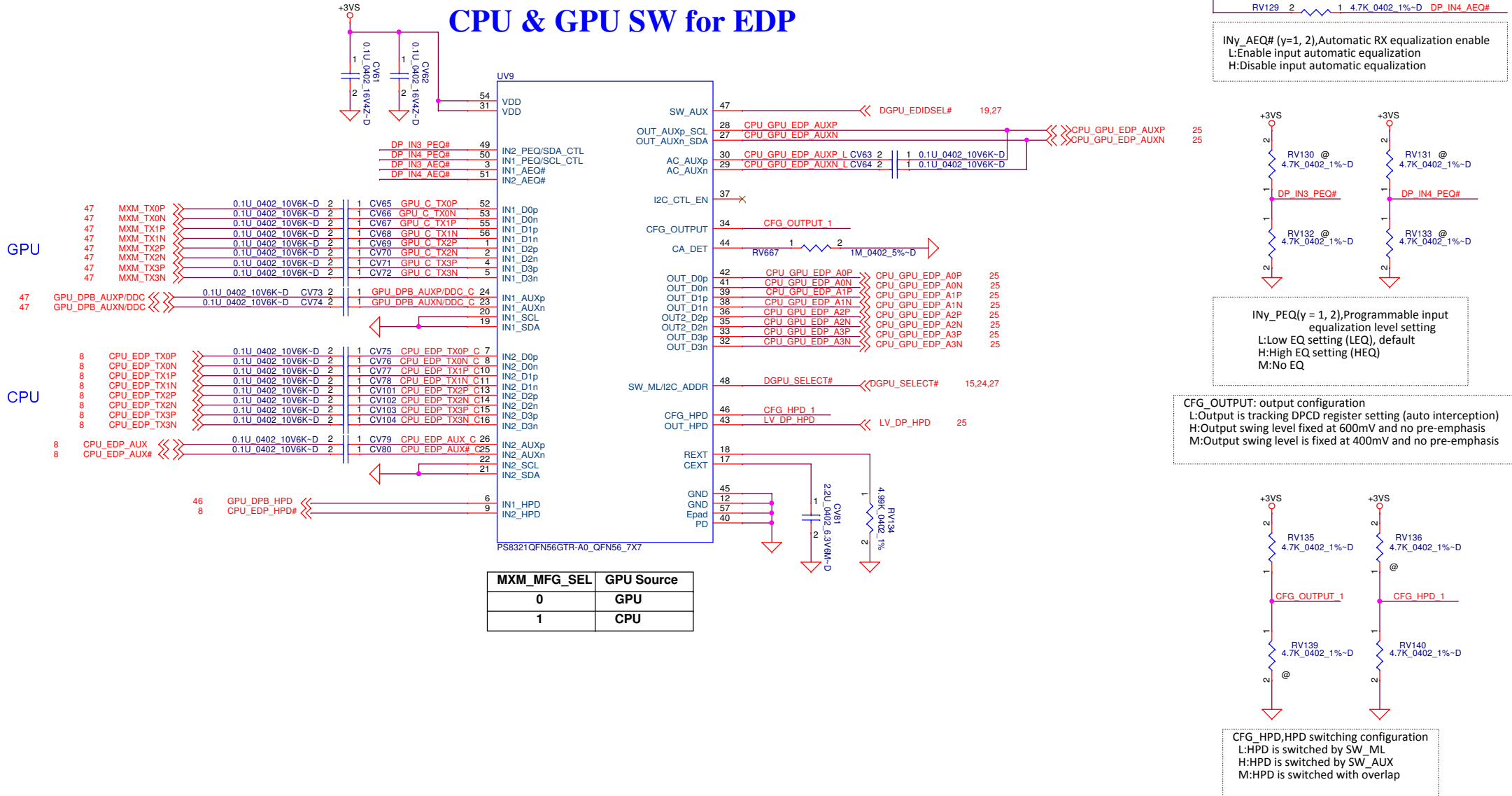
Mini DP CONN



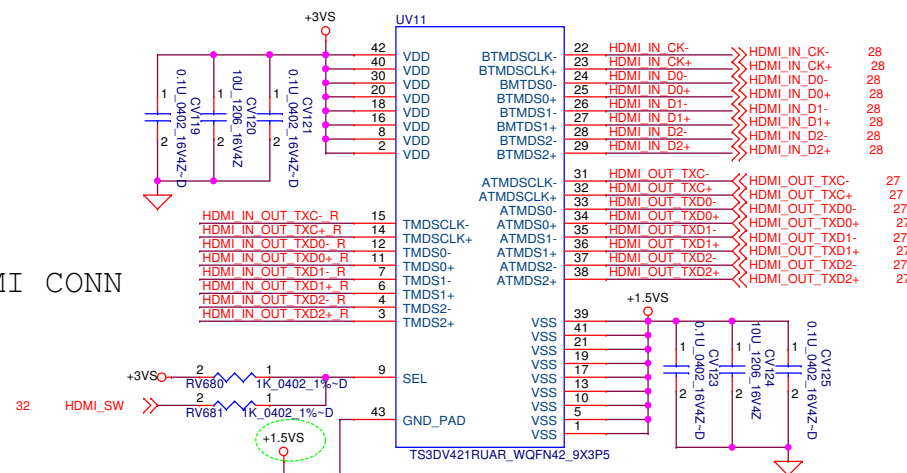
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| Issued Date | 2012/05/14 | Deciphered Date | 2013/05/13 | Compal Electronics, Inc. | |
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| | | | | Custom | LA-9201P |
| | | | | Rev | 0.1 |
| | | | | Date: | Tuesday, August 14, 2012 |
| | | | | Sheet | 23 of 66 |



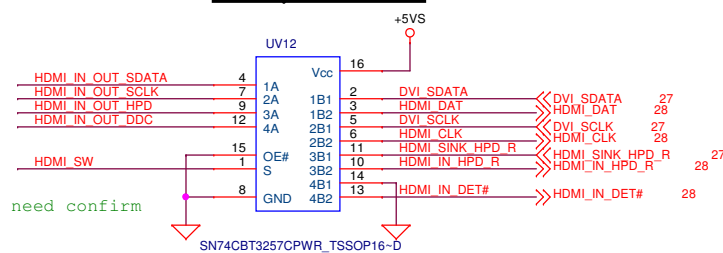
CPU & GPU SW for EDP



HDMI CONN



| SEL | OUTPUT |
|-----|--------|
| L | A |
| H | B |

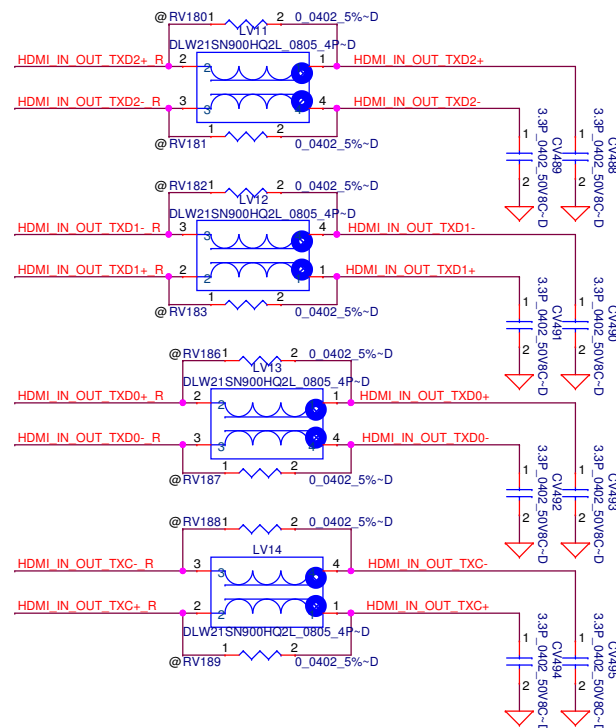


| SEL | OUTPUT |
|-----|--------|
| L | B1 |
| H | B2 |

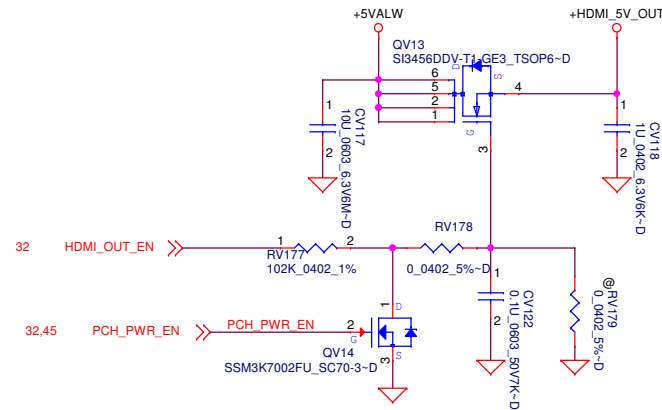
2011/11/30 need confirm
with PCH

STDP6038

CPU/GPU



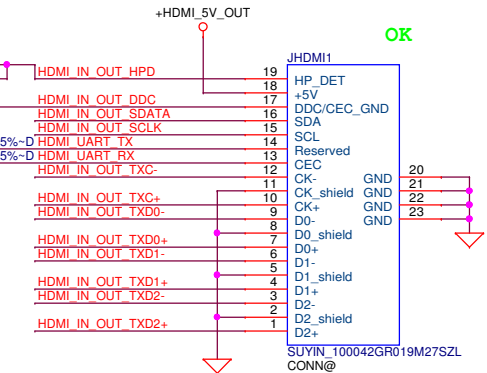
Reserve for EMI please close to JHDMI1

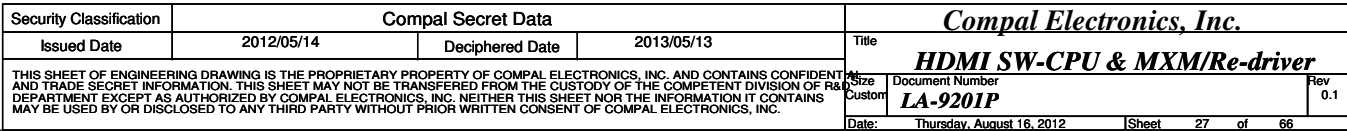


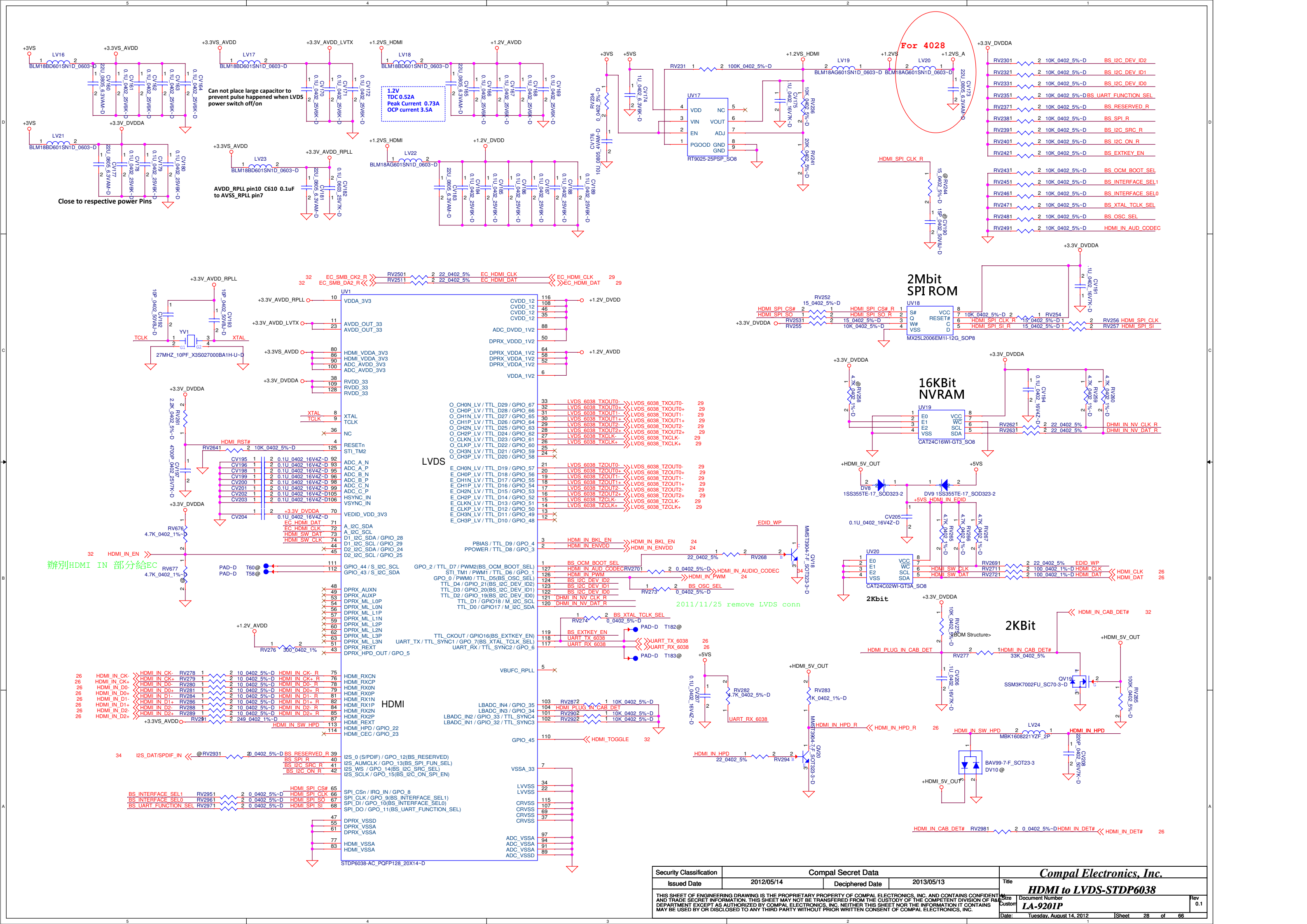
HDMI Input/Output Connector

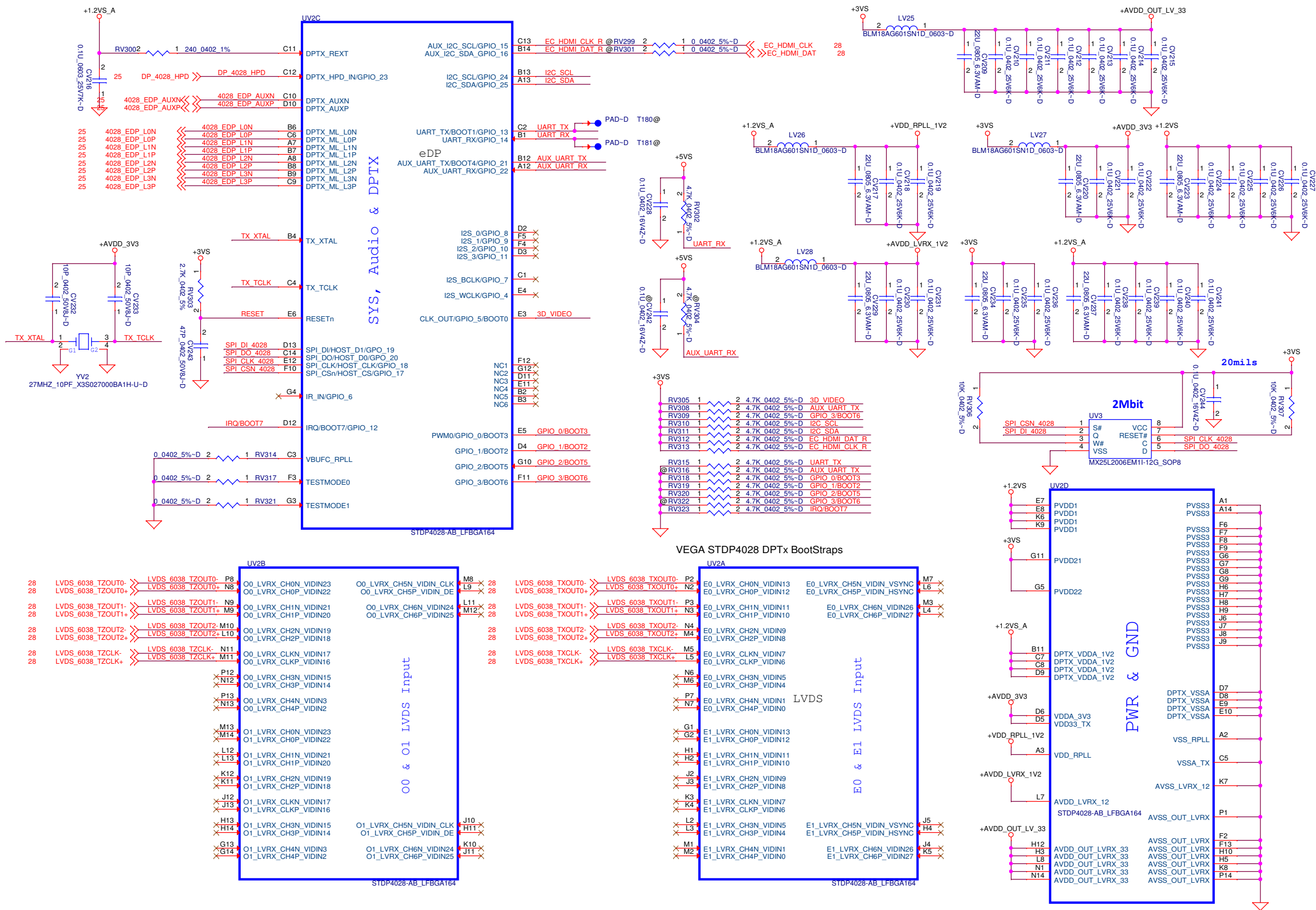
辦別HDMI IN/OUT 部分

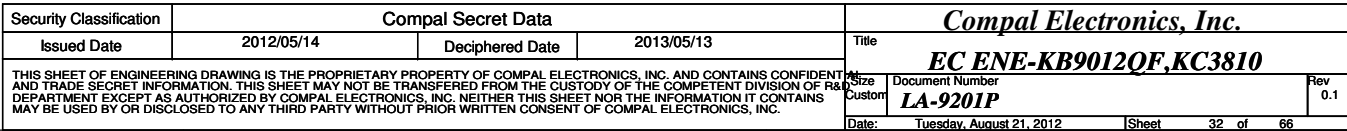
辦別HDMI IN/OUT Cable 部分

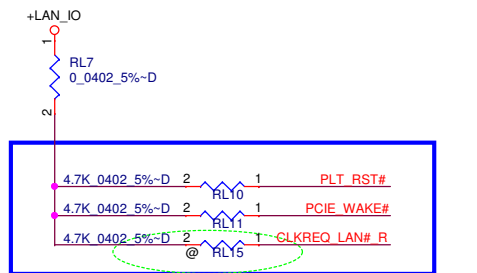




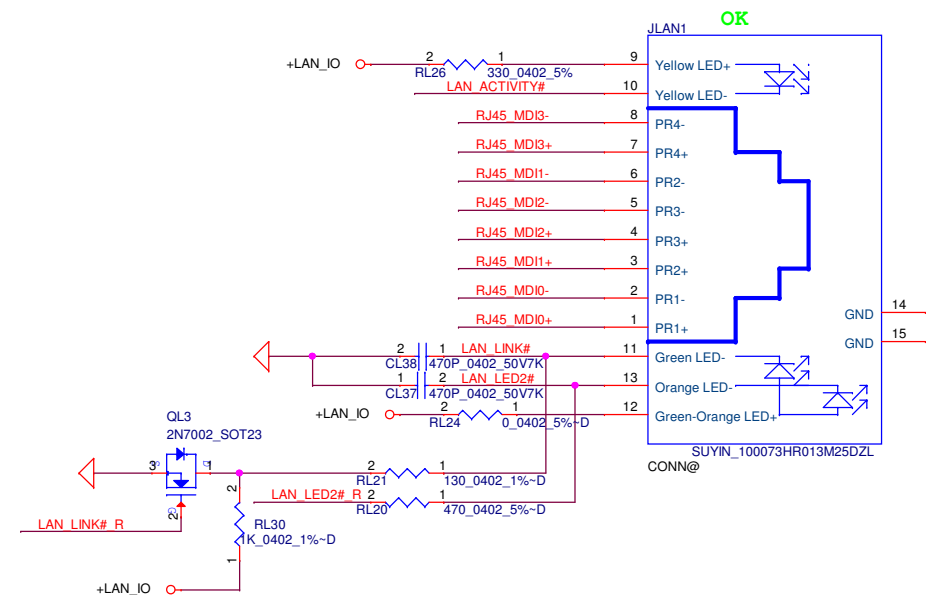
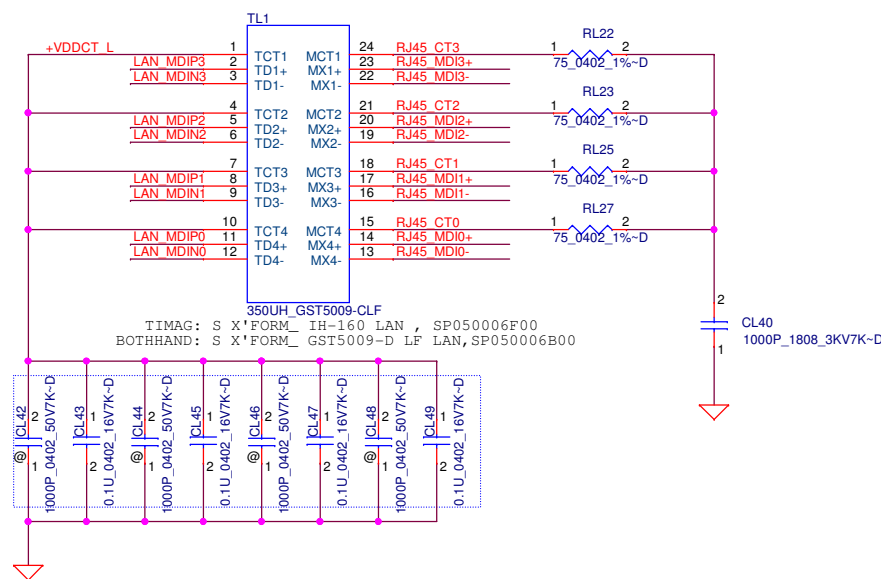
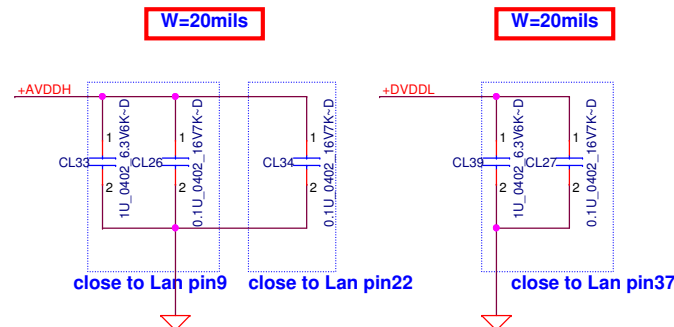
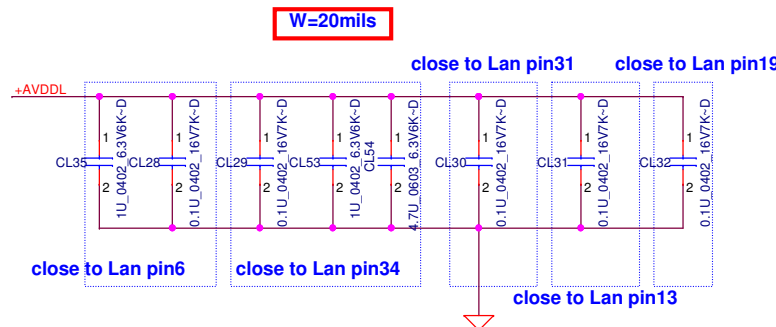
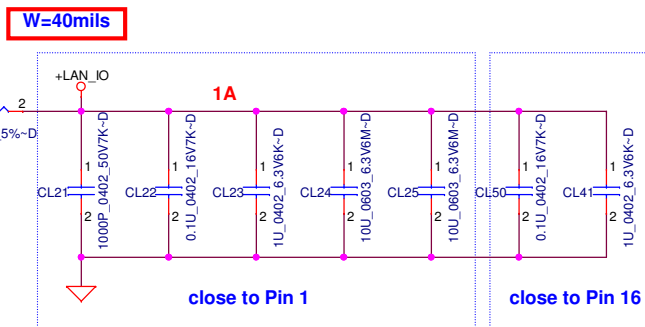
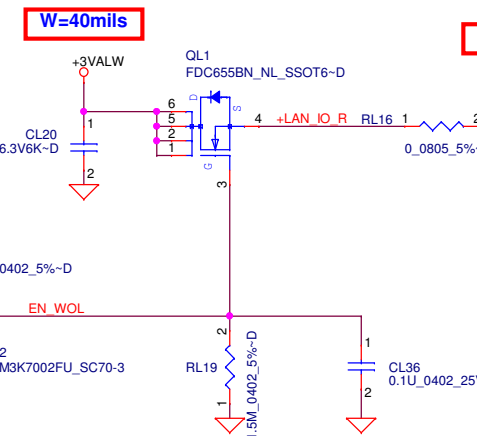
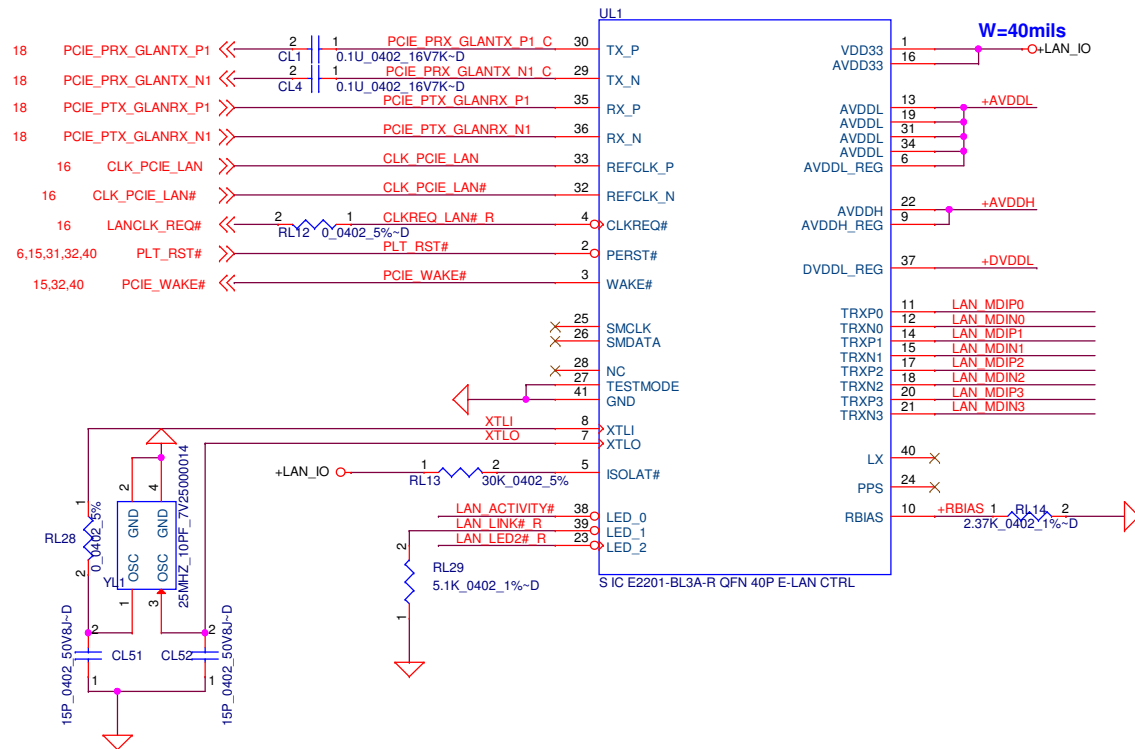




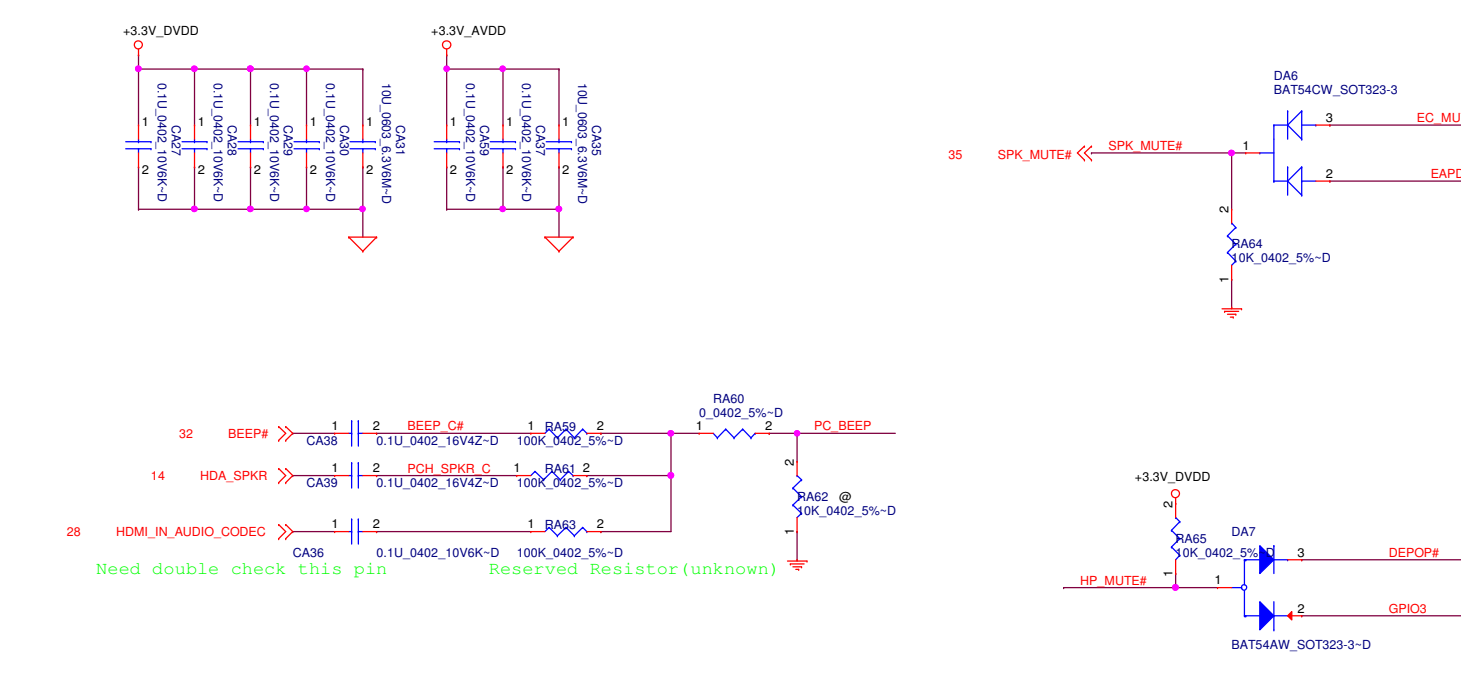
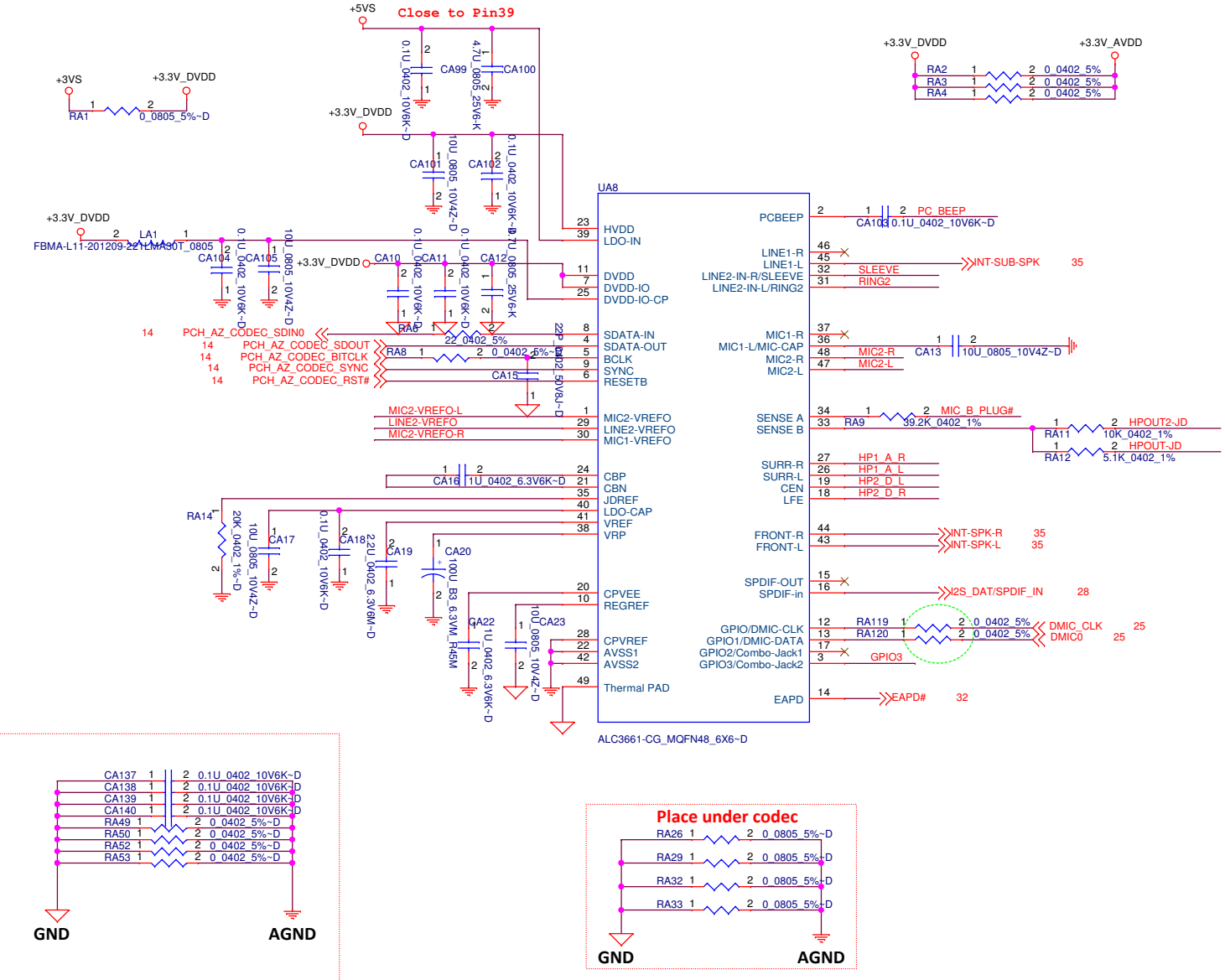




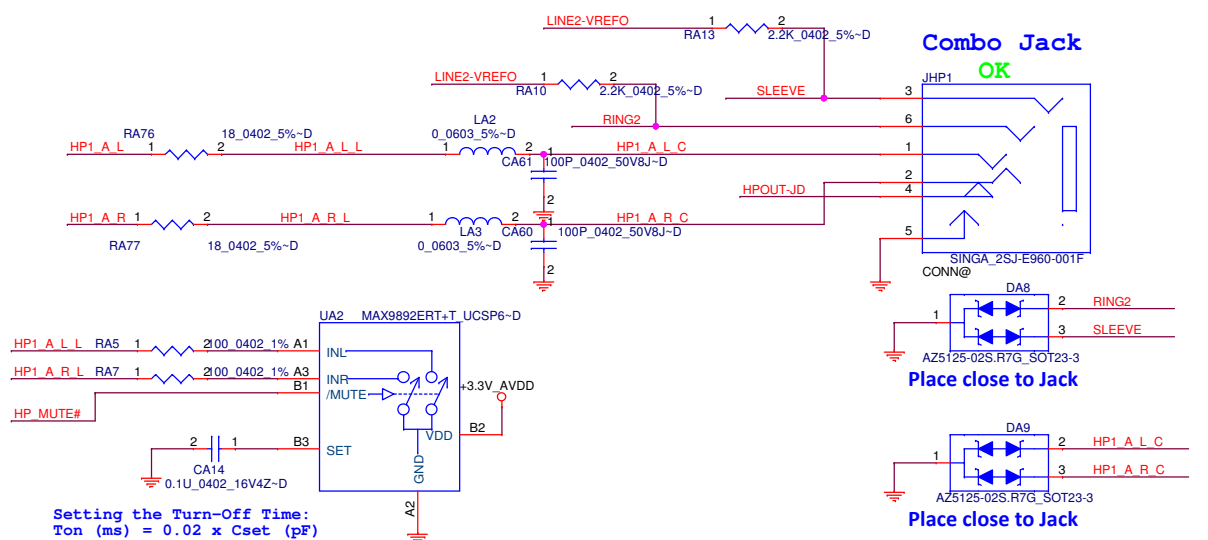
The pull-up resistors might not be necessary due to existence on PCH side.



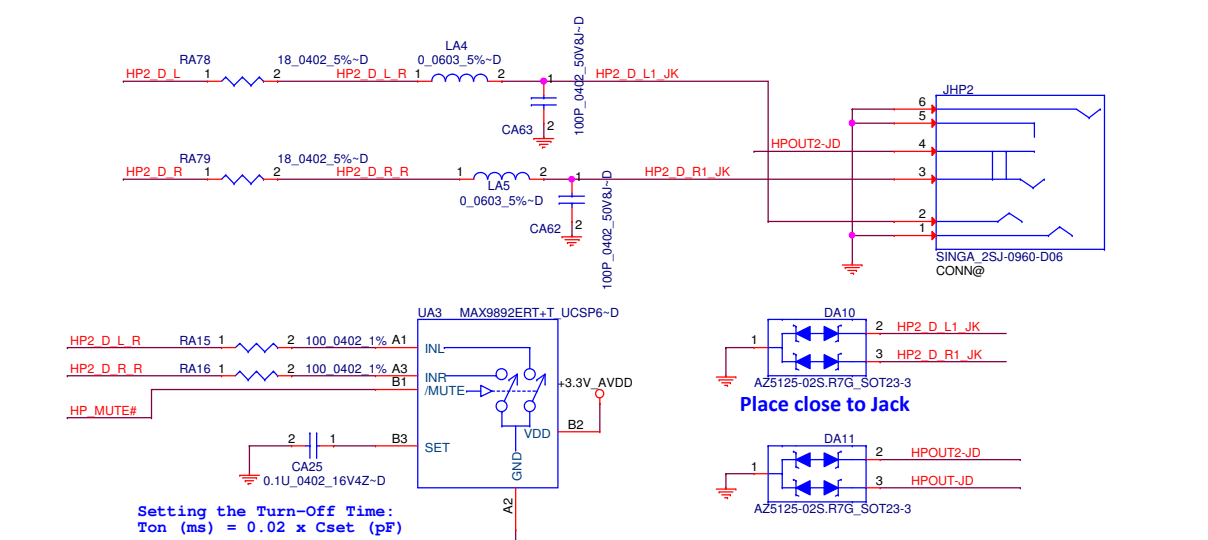
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| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2012/05/14 | Deciphered Date | 2013/05/13 | Title | GLAN AR8151 AL1A/ RJ45 |
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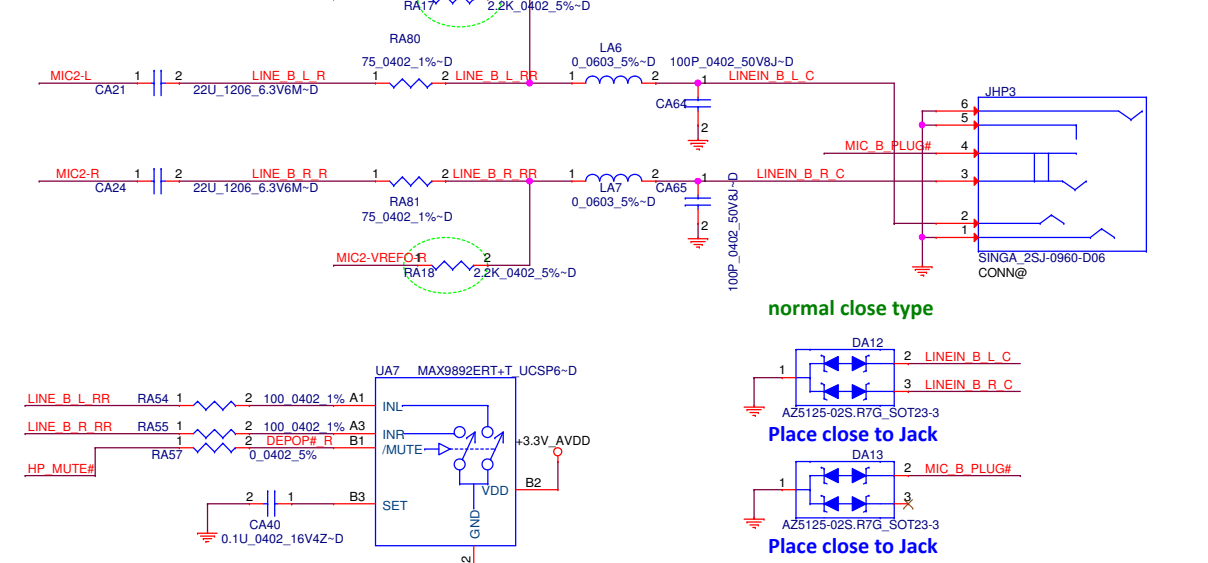
S1 (Out + In) : Front L/R + HP1 + MIC (auto-sense)

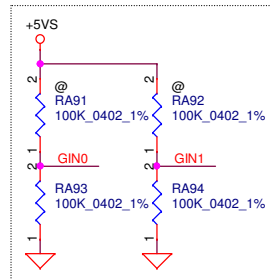
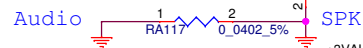


S2 (Out) :Center + HP2

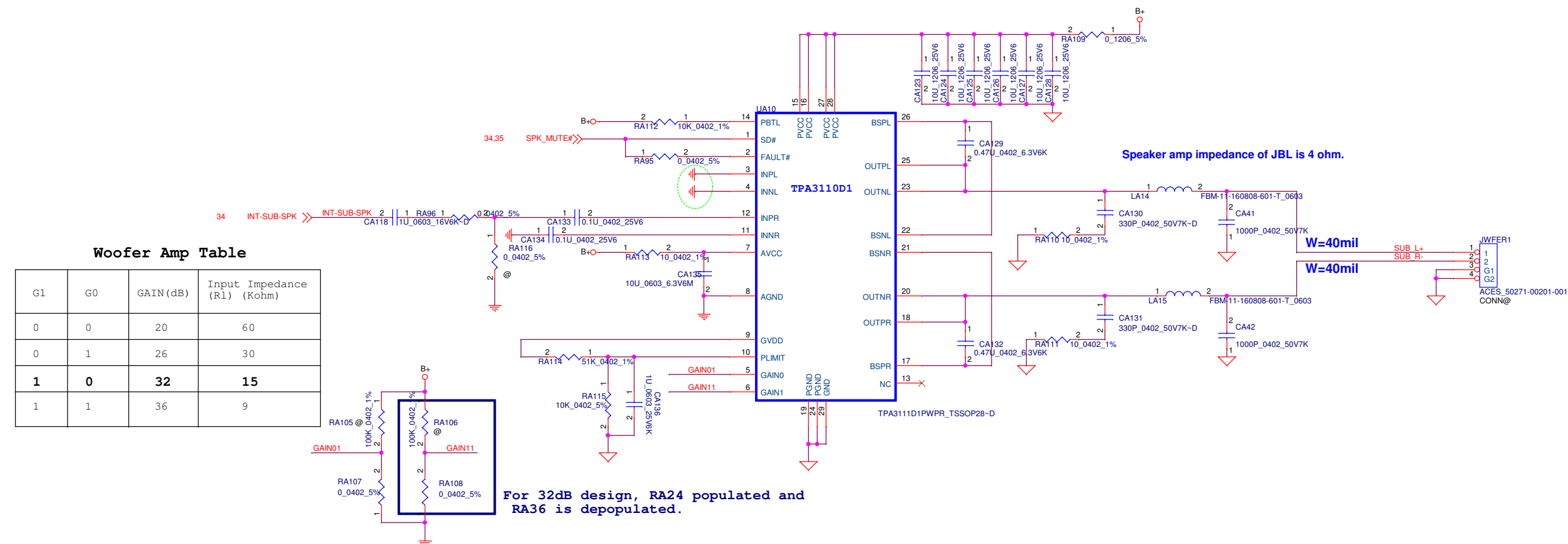
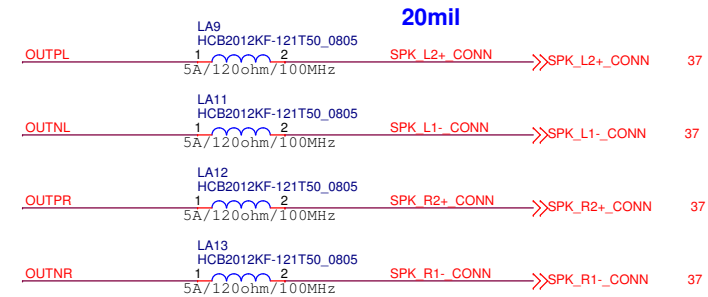
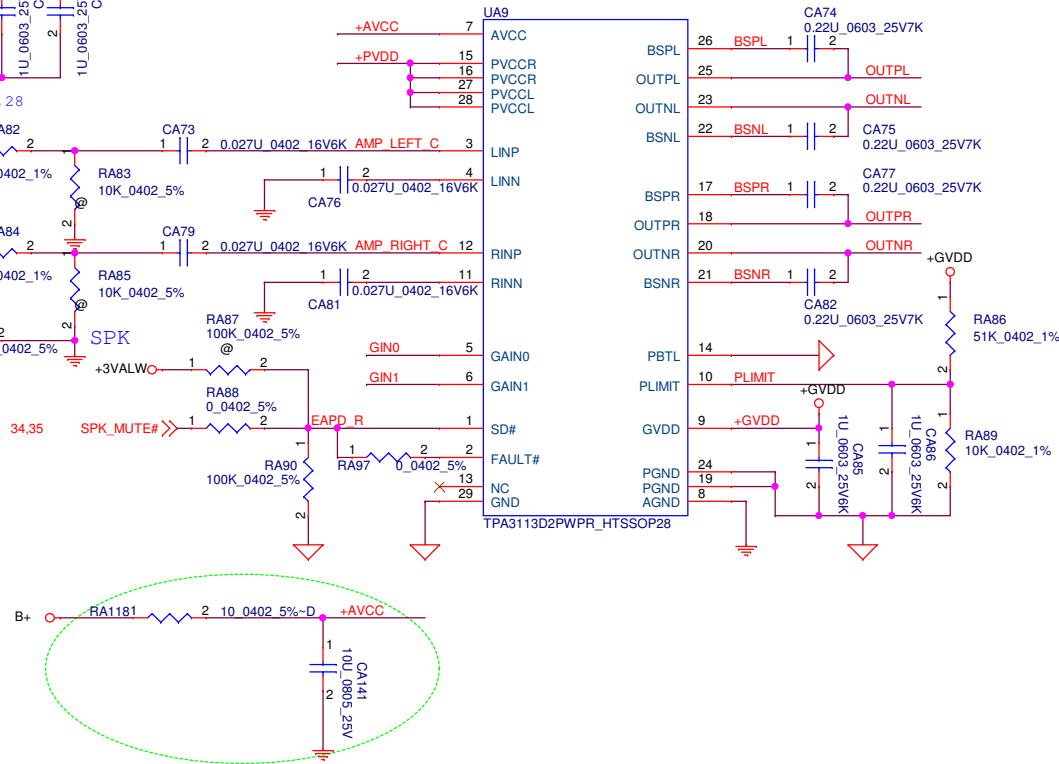


S3 (Out) : Rear L/R + MIC





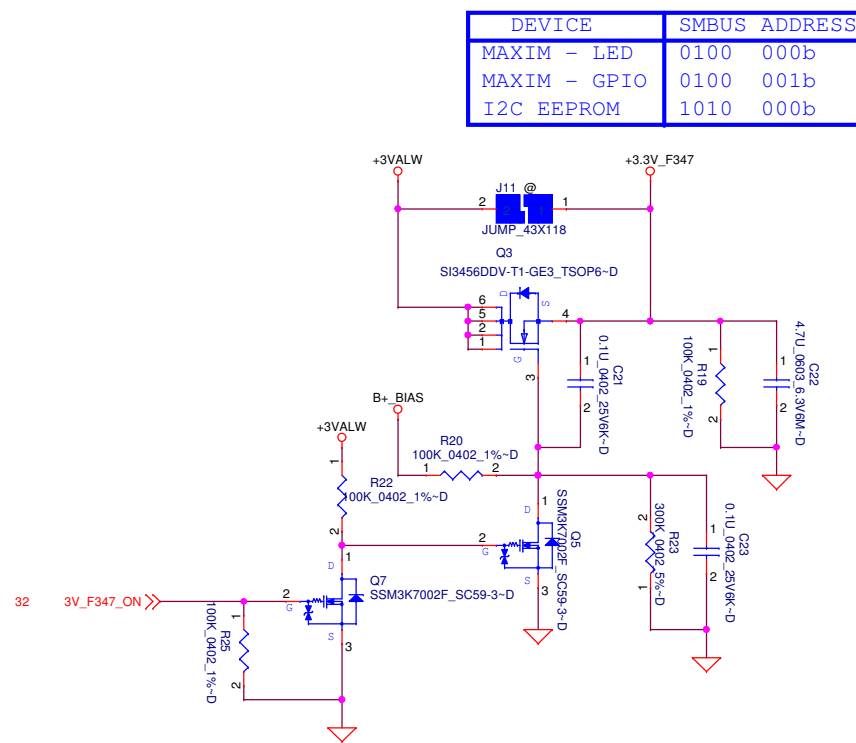
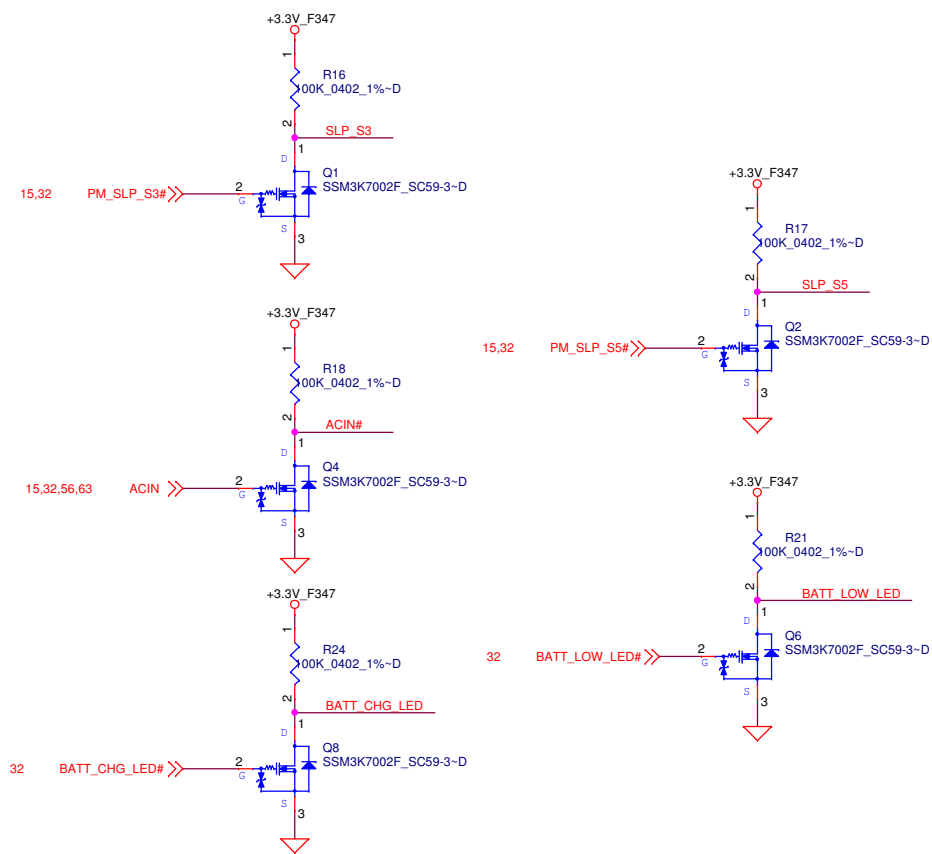
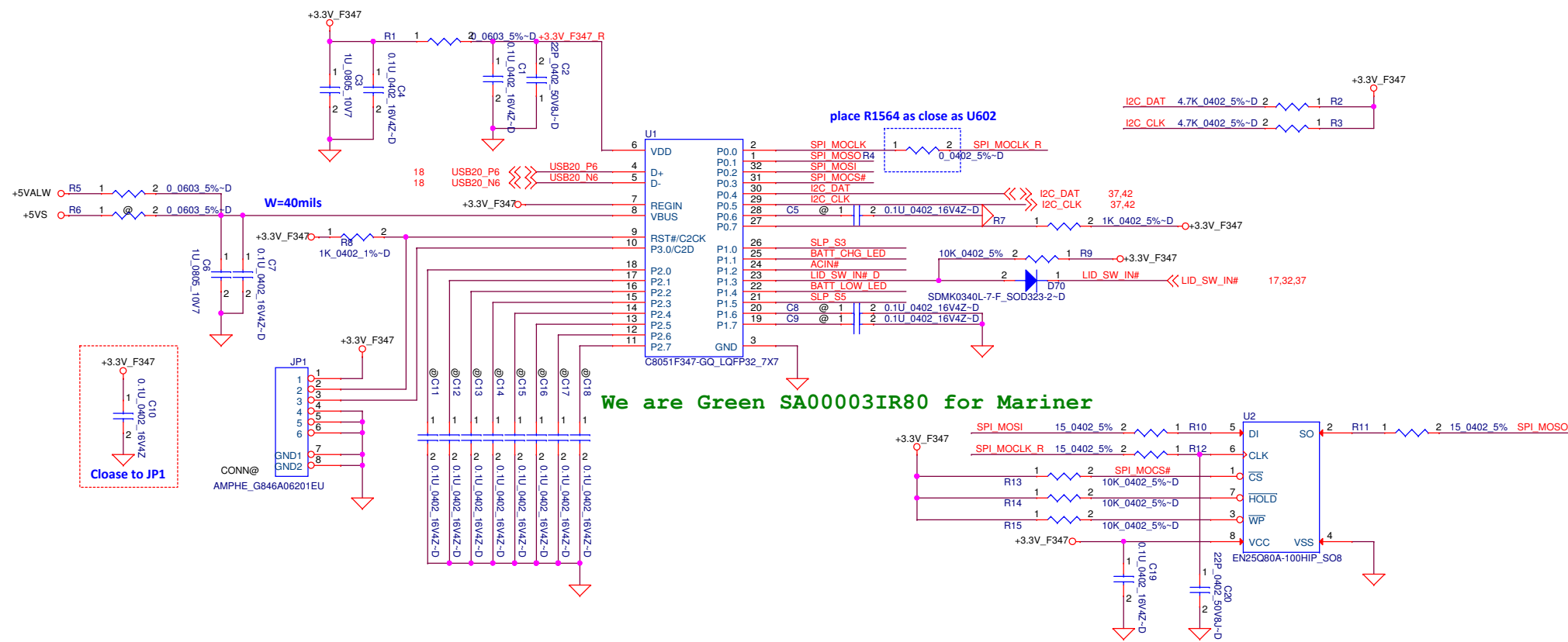
| GAIN1 | GAIN0 | AV (inv) | INPUT IMPEDANCE |
|-------|-------|----------|-----------------|
| 0 | 0 | 20dB | 60Kohm |
| 0 | 1 | 26dB | 30Kohm |
| 1 | 0 | 32dB | 15Kohm |
| 1 | 1 | 36dB | 9Kohm |



Woofers Amp Table

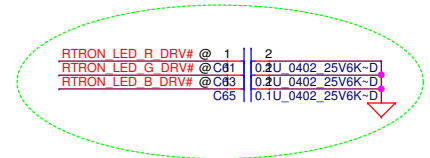
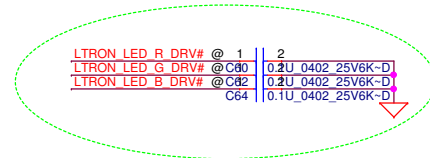
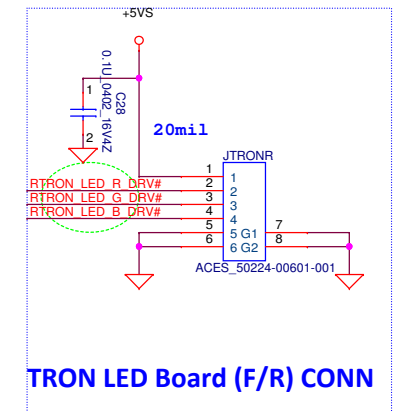
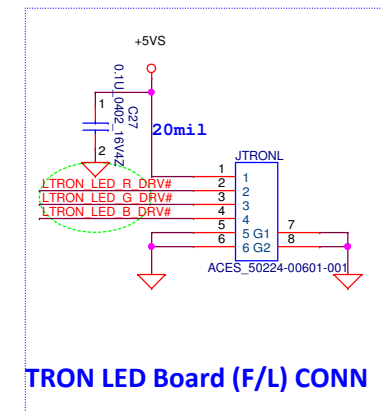
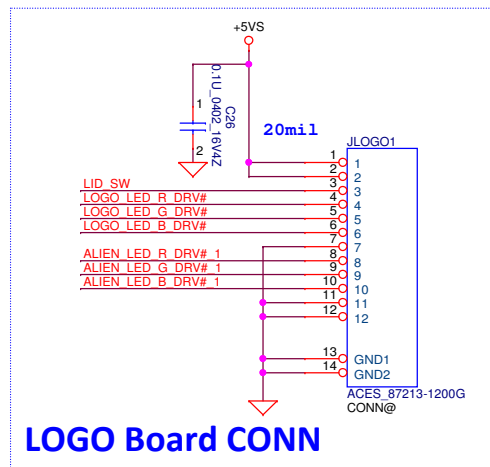
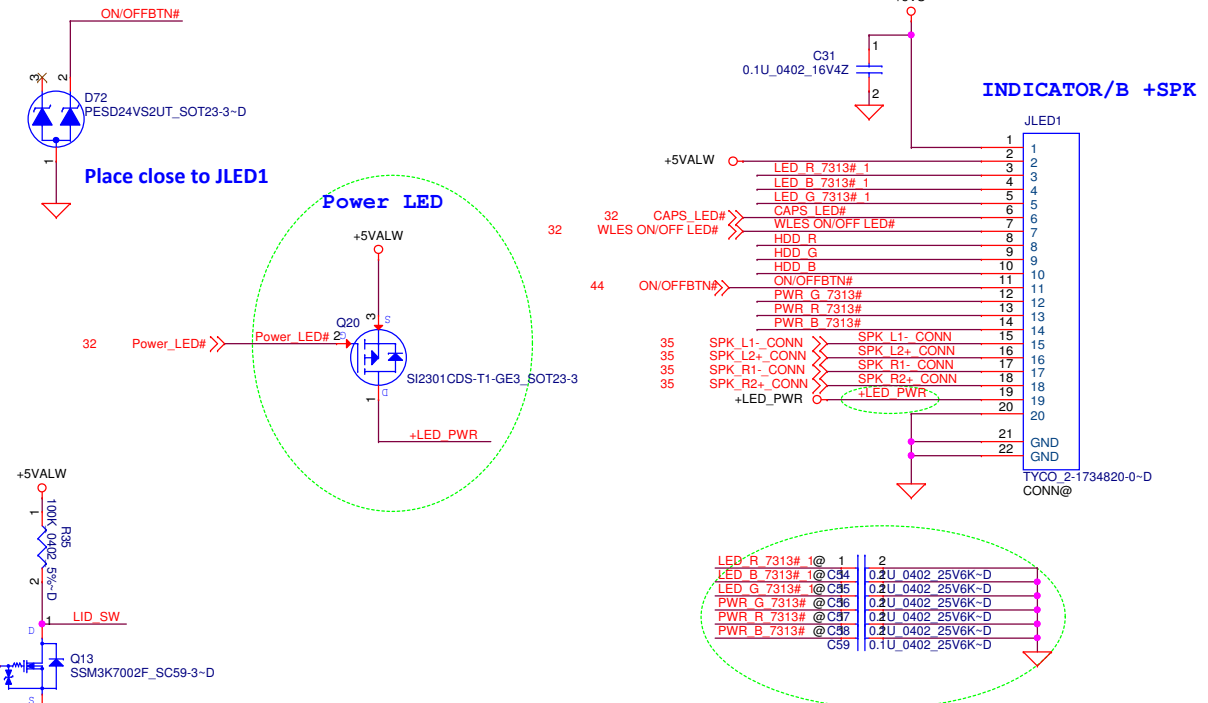
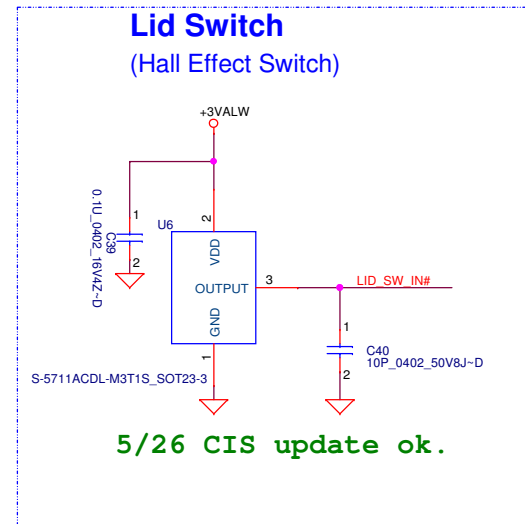
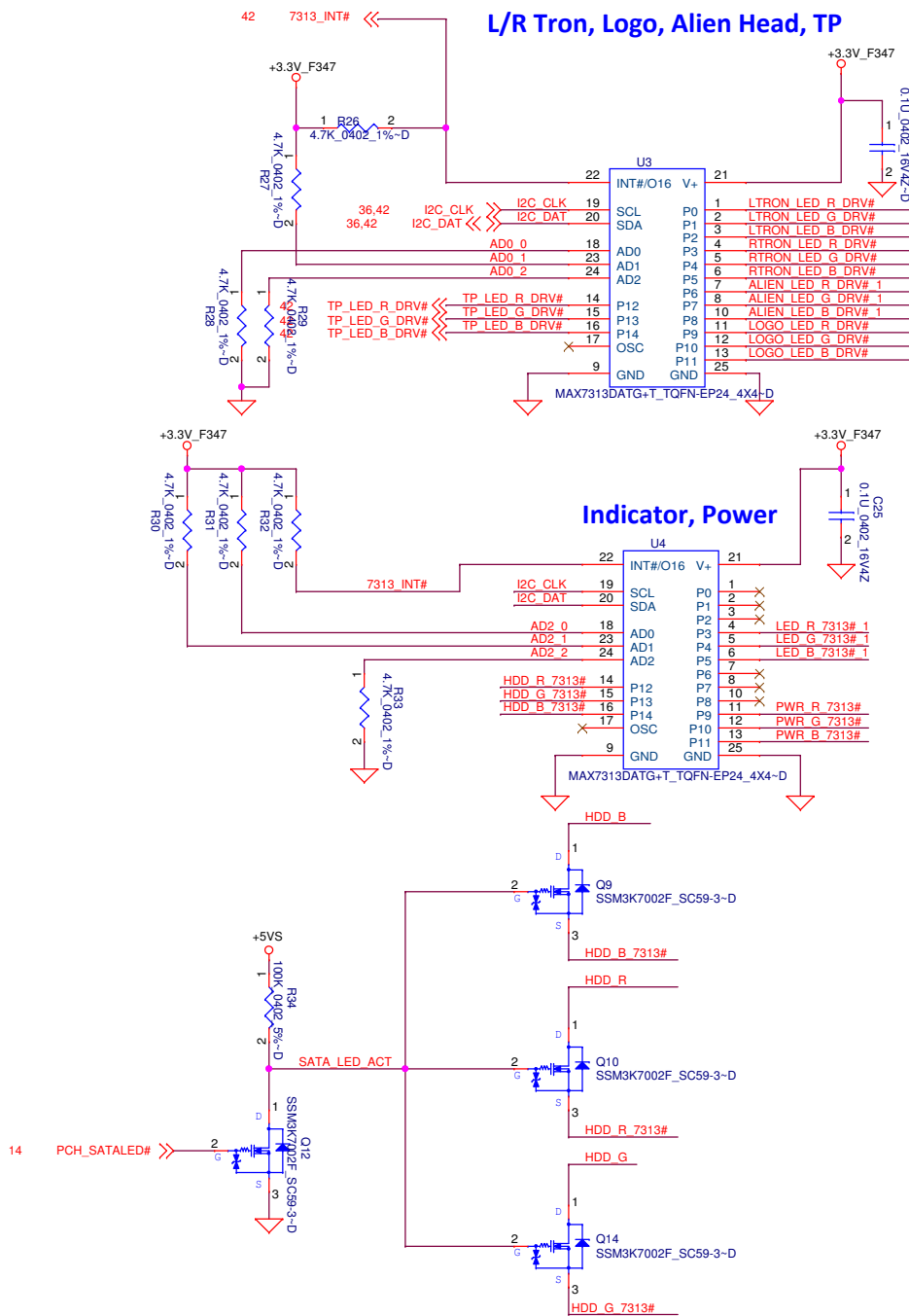
| G1 | G0 | GAIN (dB) | Input Impedance (R1) (Kohm) |
|----------|----------|-----------|--------------------------------|
| 0 | 0 | 20 | 60 |
| 0 | 1 | 26 | 30 |
| 1 | 0 | 32 | 15 |
| 1 | 1 | 36 | 9 |

For 32dB design, RA24 populated and RA36 is depopulated.

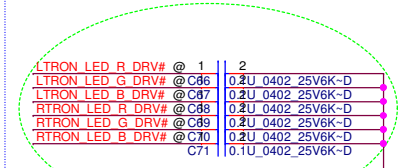
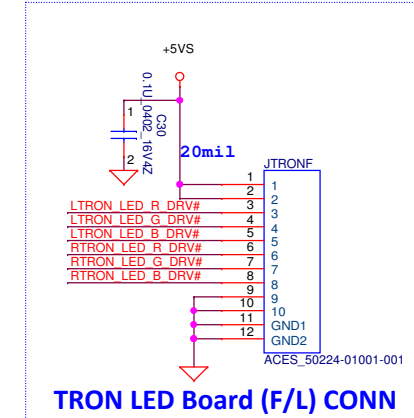
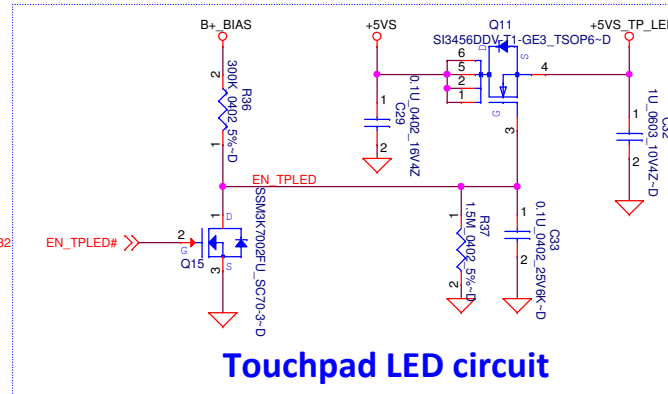
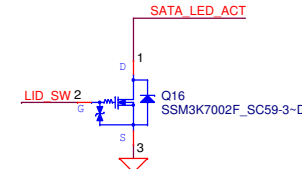


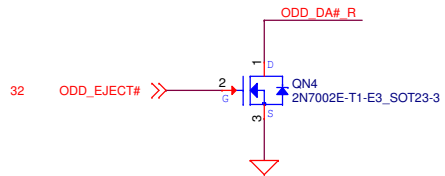
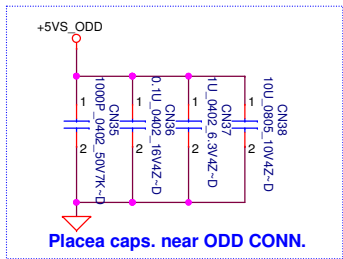
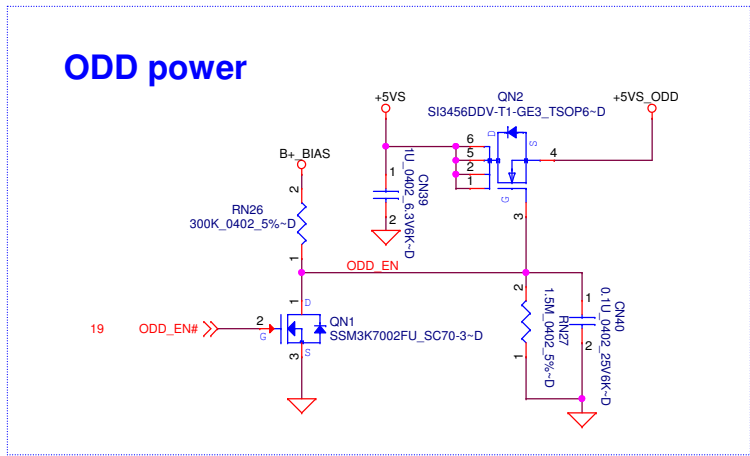
| | | +3.3V_F347 behavior | | | |
|----------|--|---------------------|----|-----|-----|
| | | STATE | | | |
| | | S0 | S3 | S4 | S5 |
| AC IN | | ON | ON | ON | ON |
| BAT only | | ON | ON | OFF | OFF |

AC mode battery full in S5:turn off ELC controller

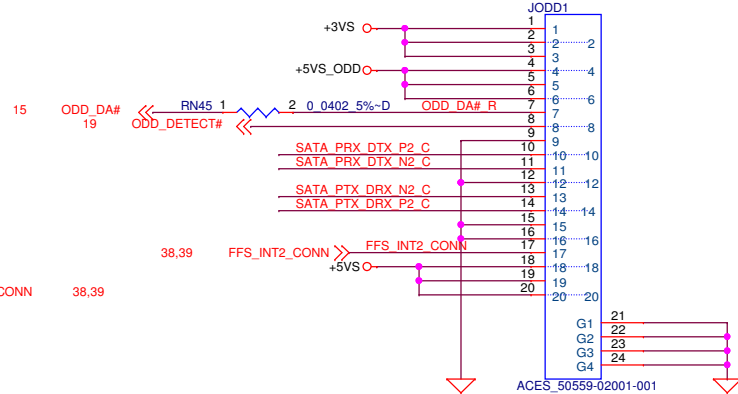


| Reference | AD2 | AD1 | AD0 | MAX7313 |
|-----------|-----|-----|-----|---|
| U605 | 0 | 1 | 0 | Tron Lights,TP A-panel,B-Panel Logo |
| U608 | 0 | 1 | 1 | Power Button, Media and Status LED Color |
| U? | 1 | 0 | 0 | Button, Indicator Brightness |

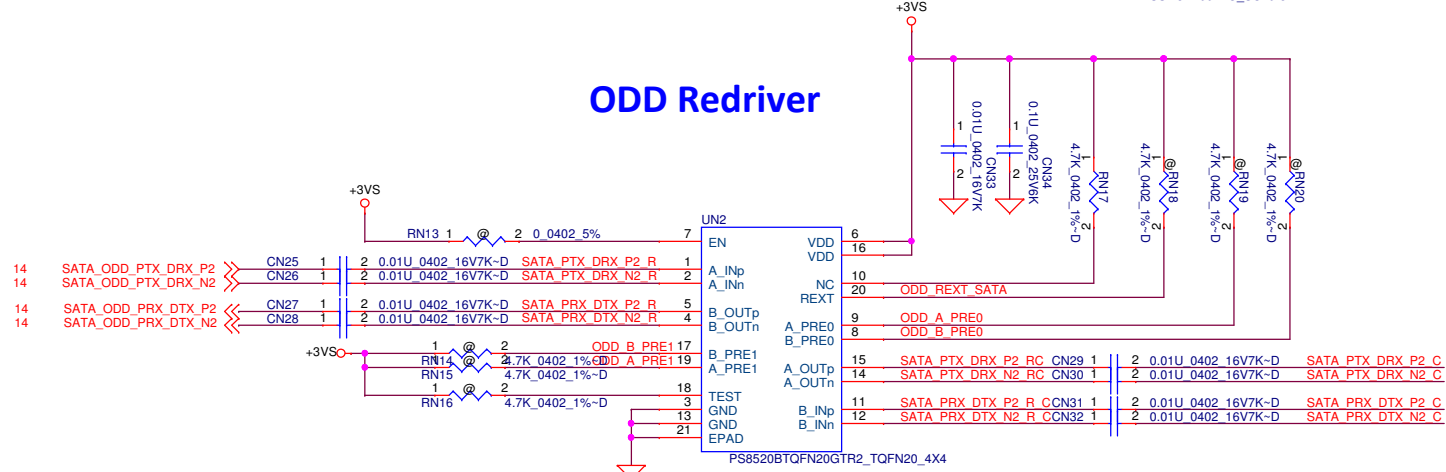




SATA ODD Conn.



ODD Redriver



- ODD_B_PRE0 RN21 1 @ 2 0 0402 5%
- ODD_B_PRE1 RN22 1 @ 2 0 0402 5%
- ODD_A_PRE1 RN23 1 @ 2 0 0402 5%
- ODD_A_PRE0 RN24 1 @ 2K 0402 5%
- ODD_REXT_SATA RN25 @ 5.1K 0402 1%

Pin 20:
PARADE PS8250B:
depop RN18, RN25

PERICOM PI3EQX6741ST:
pop RN18, depop RN25

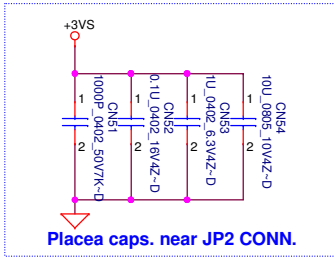
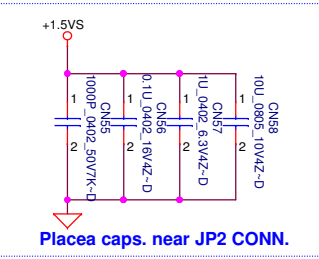
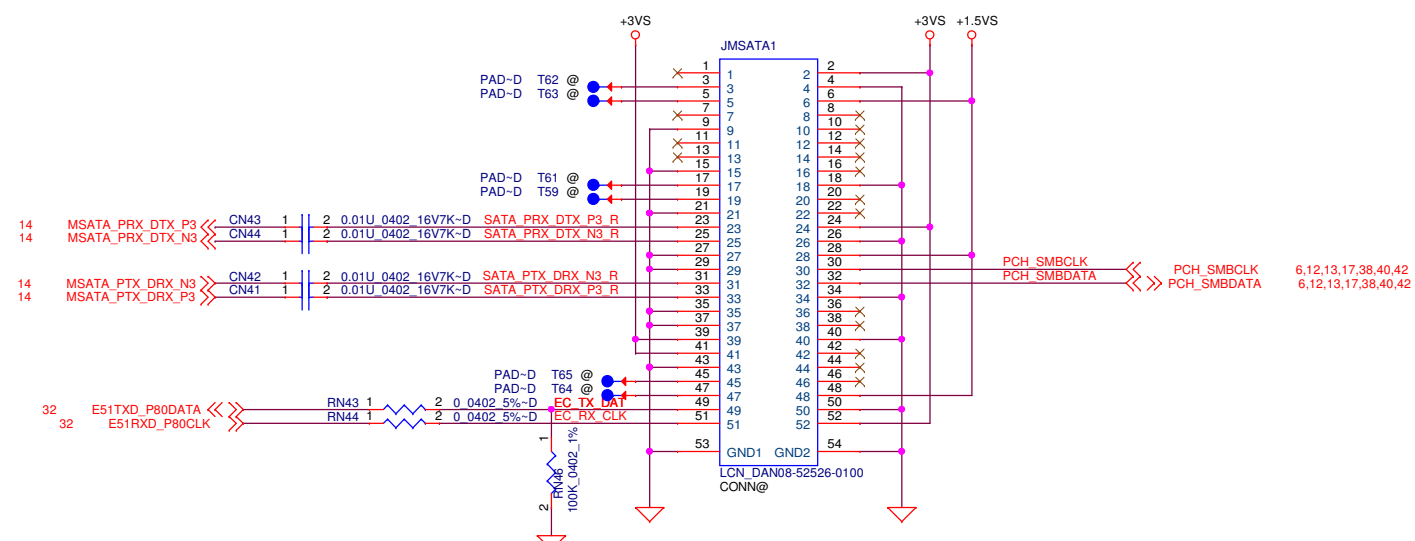
ASMEDIA ASM1466:
pop RN18, depop RN25

Pin 9:
PARADE PS8250B:
depop RN24.

PERICOM PI3EQX6741ST:
depop RN24

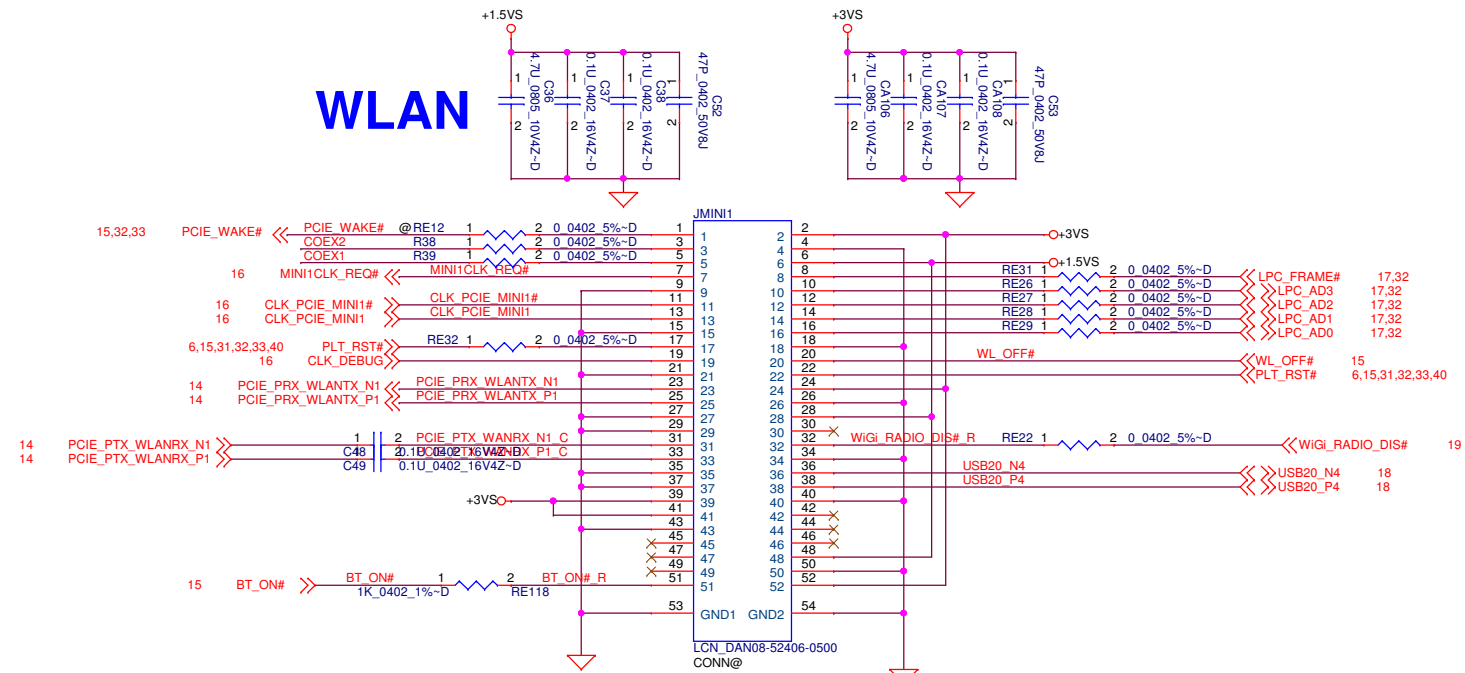
ASMEDIA ASM1466:
pop RN24 to pull down

m-SATA CONN

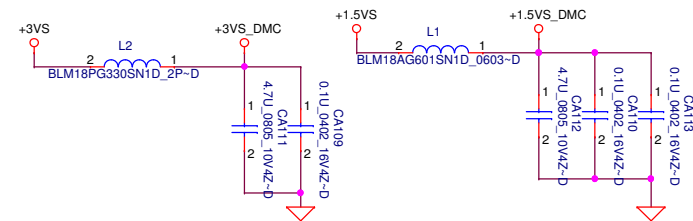
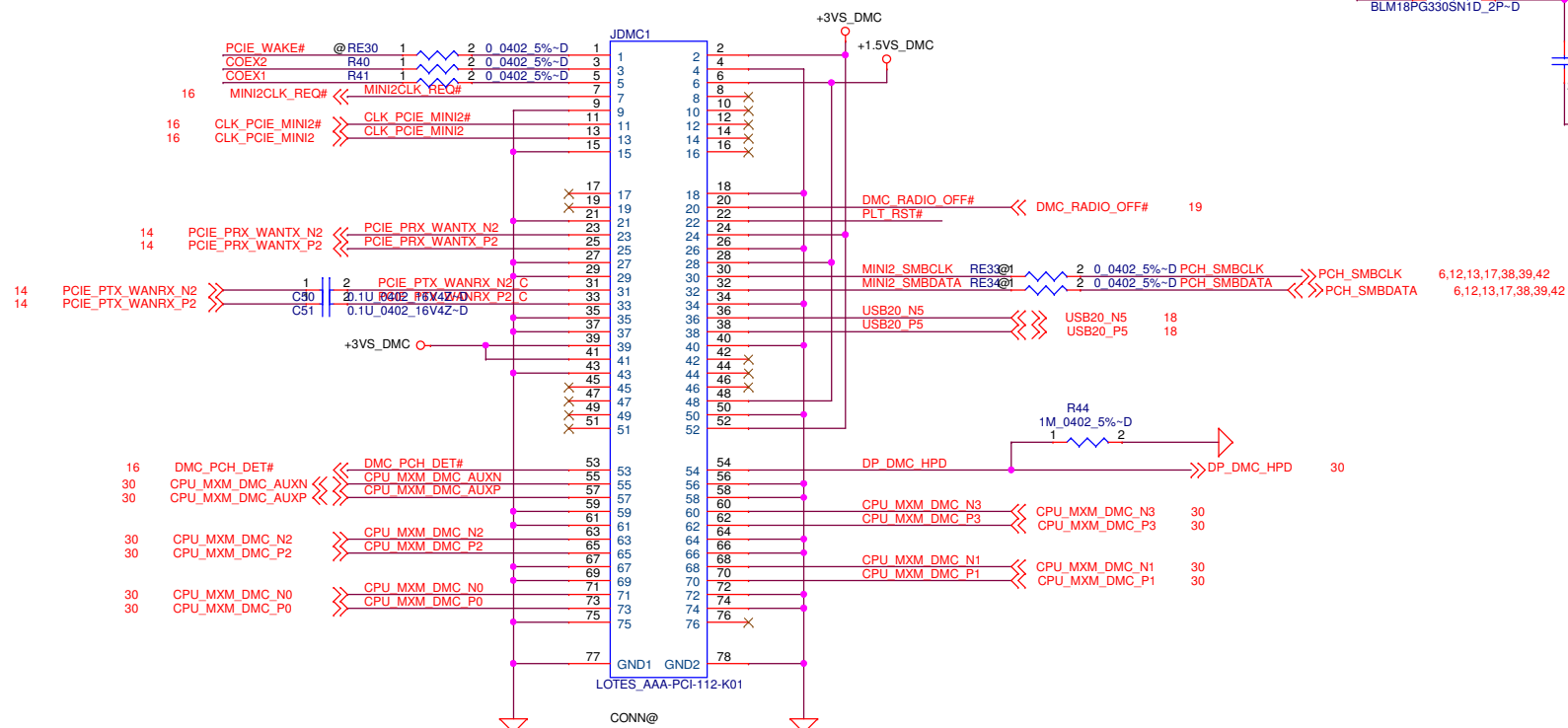


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|---|--------------------|-----------------|------------|--------------------------|
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| Date: Thursday, August 16, 2012 | | | | Rev 0.1 |
| Sheet 39 of 66 | | | | |

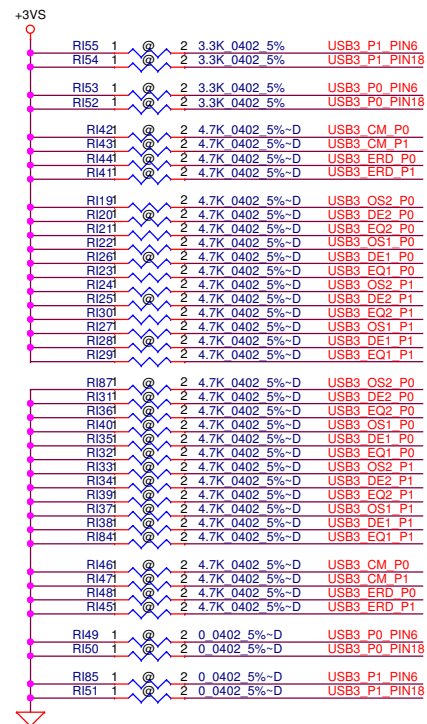
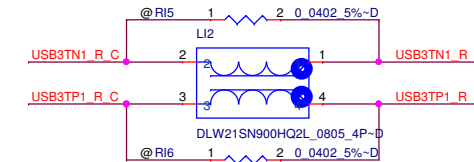
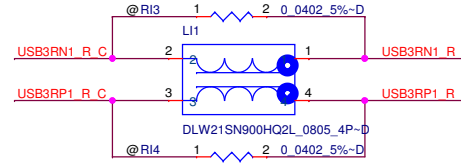
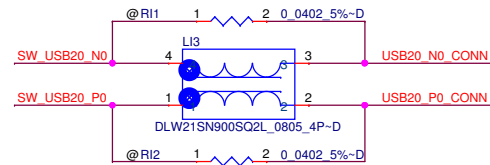
WLAN



Display Mini Card (DMC)

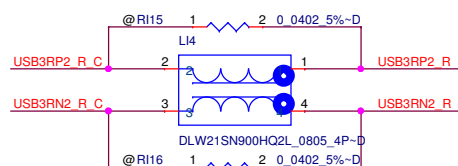
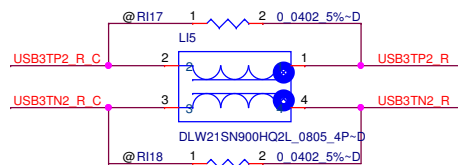
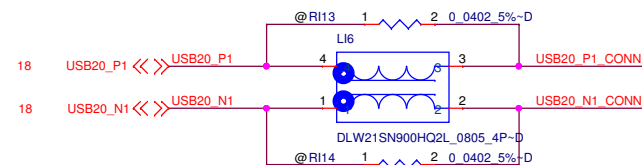


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| Issued Date | 2012/05/14 | Deciphered Date | 2013/05/13 | Title | <i>Mini Card -WLAN/DMC/BT</i> | |
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| | | | | Custom | LA-9201P | 0.1 |
| Date: | | | | Thursday, August 16, 2012 | Sheet | 40 of 66 |

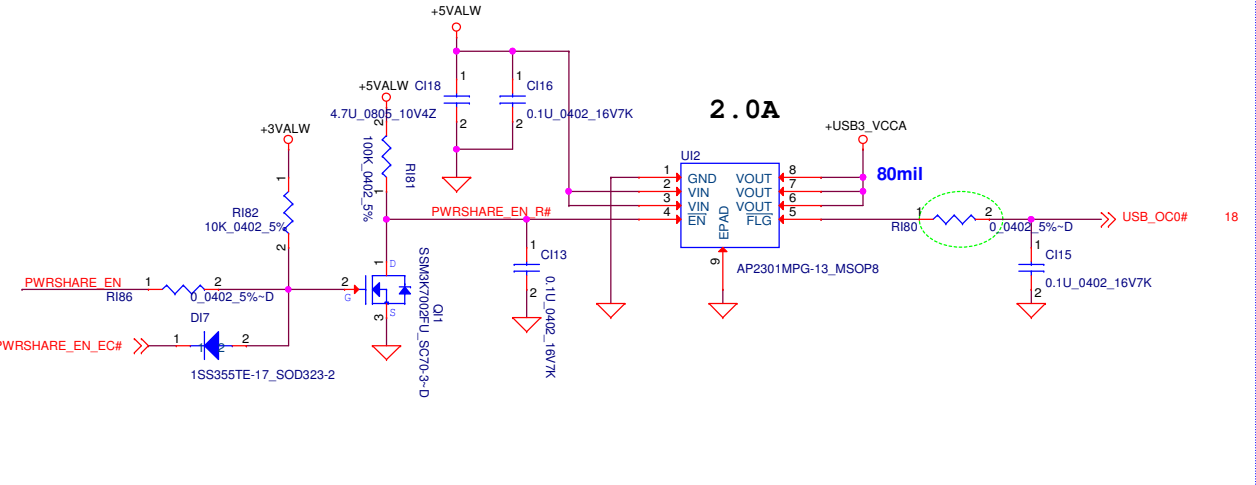
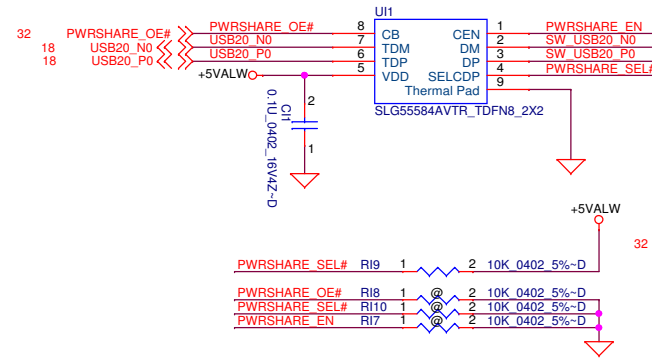


| Vendor pin | PS8710B (default) | TI |
|------------|-------------------|--------|
| pin15 | AEQ1 | OS2 |
| pin16 | ADE0 | DE2 |
| pin17 | AEQ0 | EQ2 |
| pin4 | BEQ1 | OS1 |
| pin3 | BDE0 | DE1 |
| pin2 | BEQ0 | EQ1 |
| pin5 | PD | EN_RXD |
| pin14 | TEST | CM |
| pin18 | ADE1 | |
| pin6 | BDE1 | |

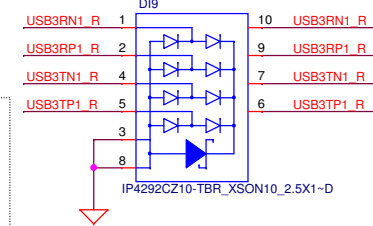
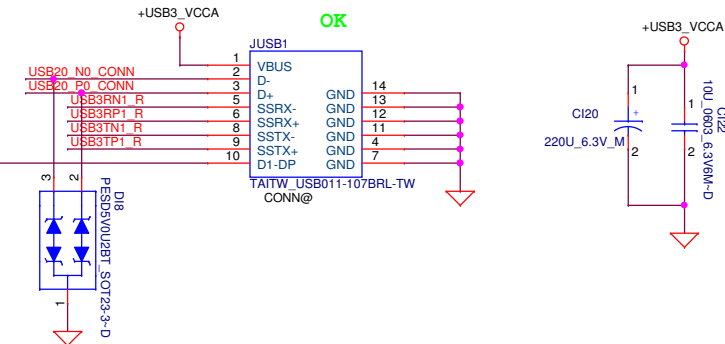
[Parade suggest]
PS8710 AEQ0,BEQ0 adjust 7db,
REXT use 3.3 K well get btter test result.



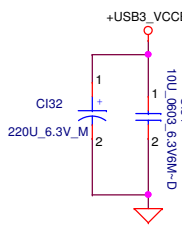
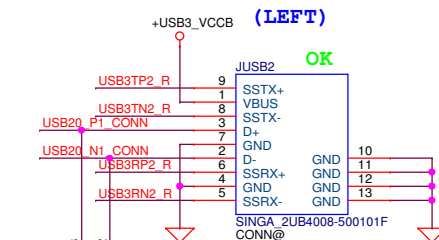
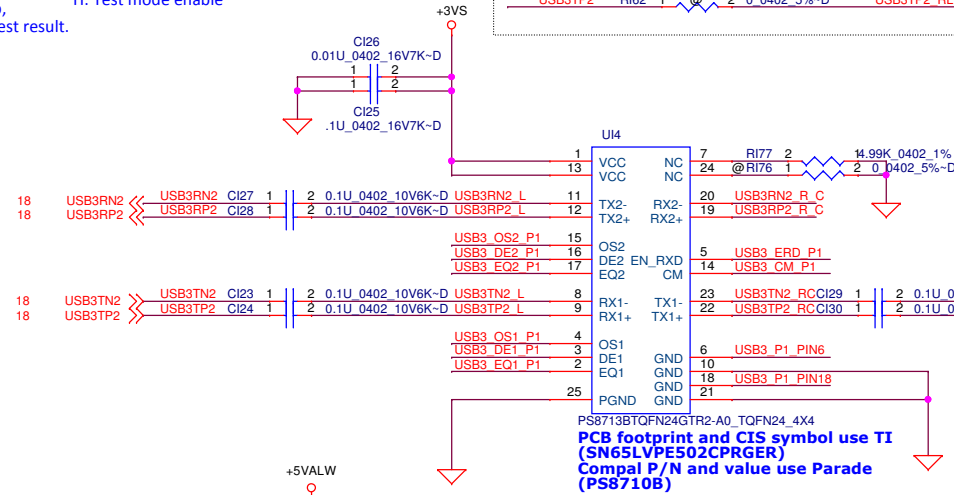
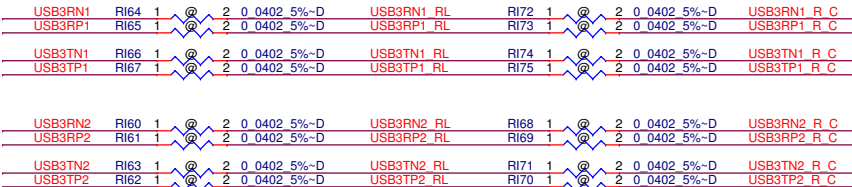
Power share

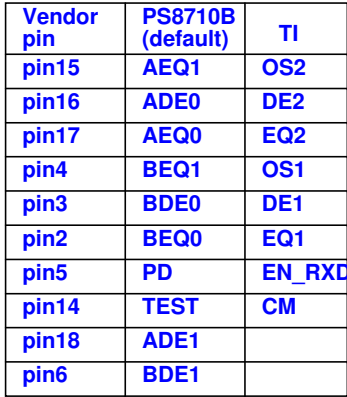


Power share USB CONN



For OPTION reserve



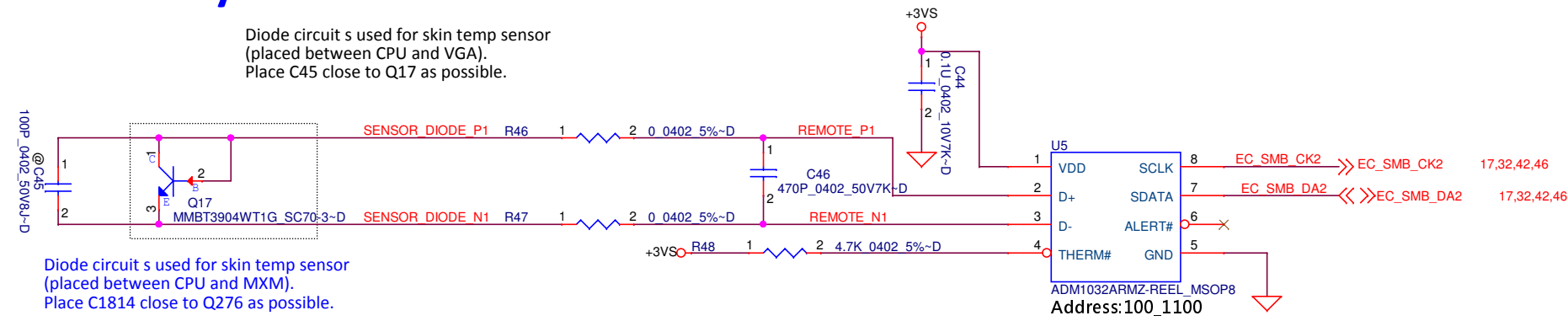


[Parade suggest]
PS8710 AEQ0,BEQ0 adjust 7db,
REXT use 3.3 K will get better test result.

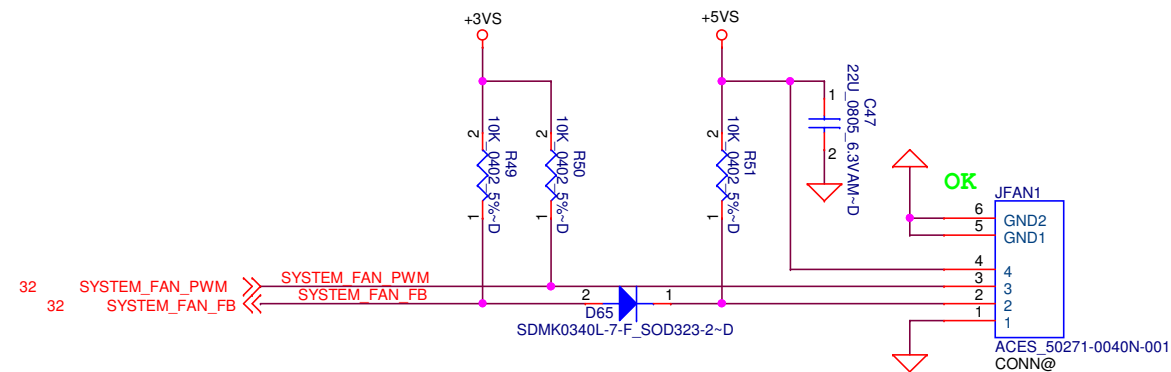
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| Security Classification | | Compal Secret Data | | | |
| Issued Date | 2012/05/14 | Deciphered Date | 2013/05/13 | Title | USB & IO CONN |
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| | | | | Document Number | 0.1 |
| | | | | LA-9201P | |
| Date: | Thursday, August 16, 2012 | Sheet | 42 | of | 66 |

System FAN Controller

Diode circuit s used for skin temp sensor
(placed between CPU and VGA).
Place C45 close to Q17 as possible.

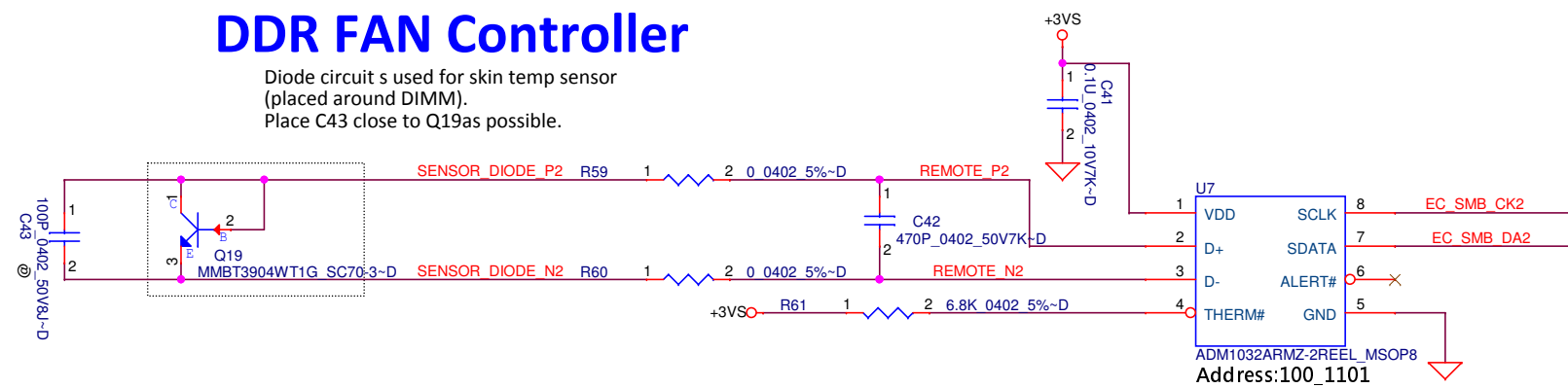


| Pull up resistor on thermtrip pin | SMBUS address |
|--------------------------------------|---------------|
| 4.7k | 1111 |
| 6.8k | 1011 |
| 10k | 1001 |
| 15k | 1101 |
| 22k | 0011 |
| 33k | 0111 |

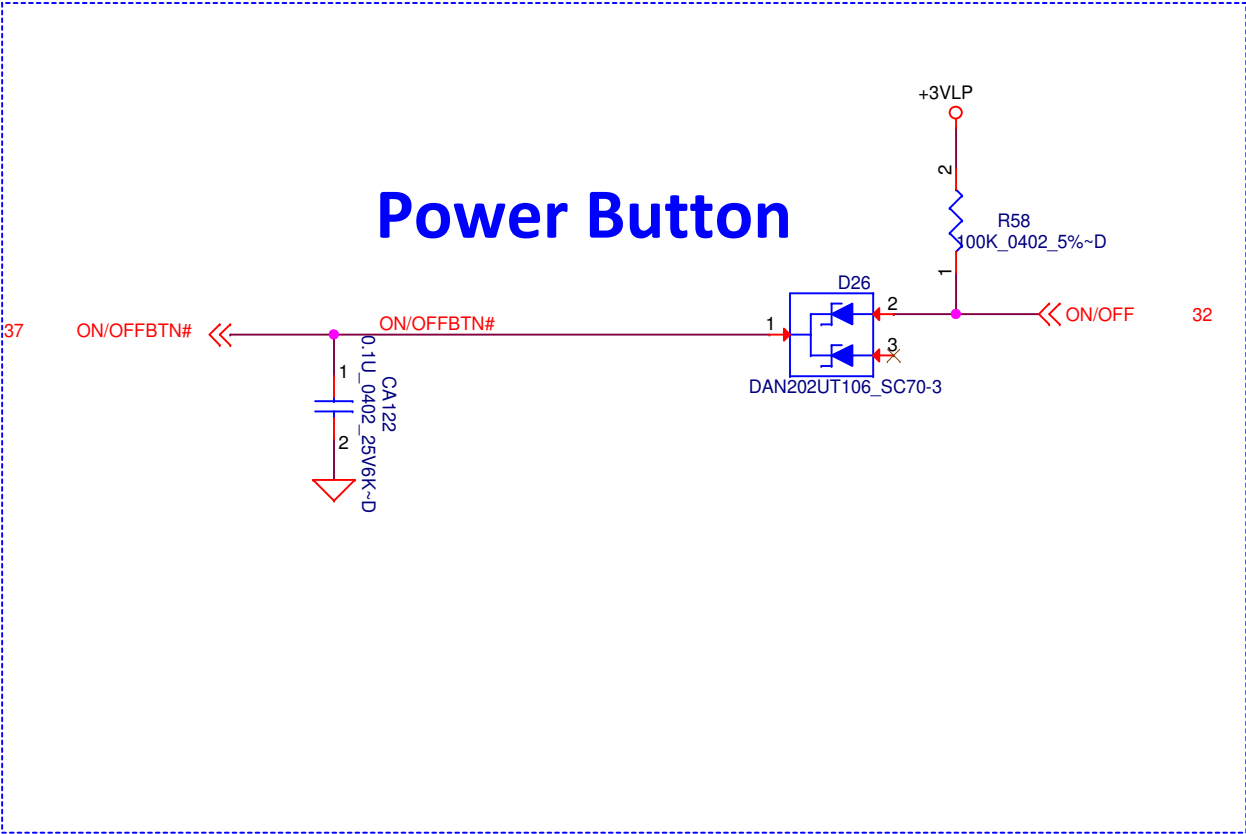
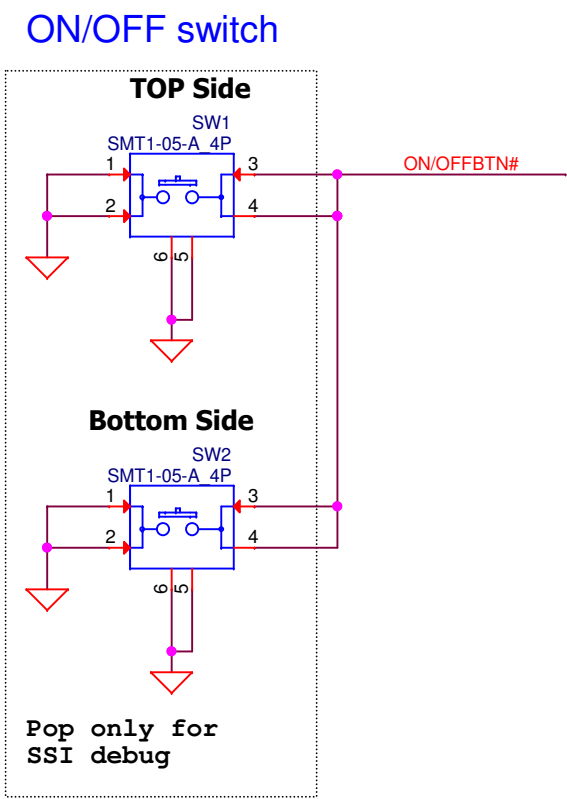
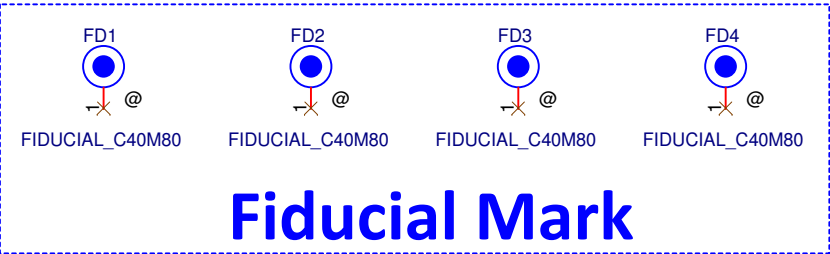
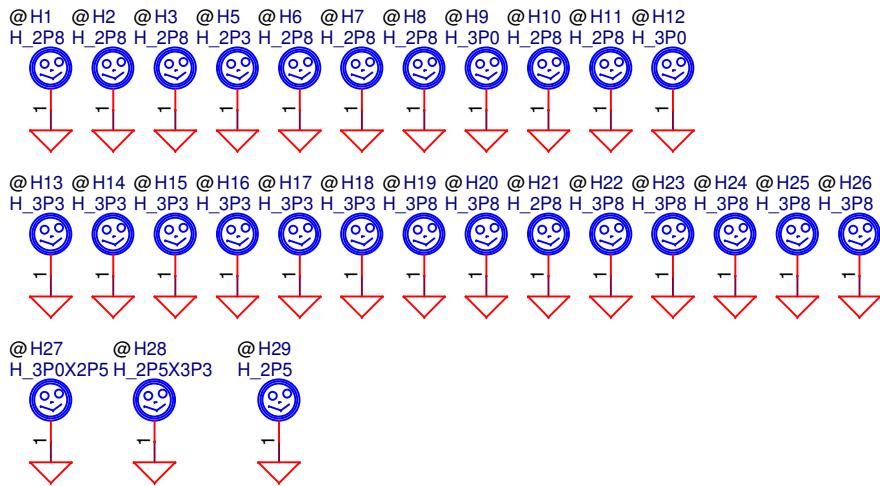


DDR FAN Controller

Diode circuit s used for skin temp sensor
(placed around DIMM).
Place C43 close to Q19as possible.



| | | | | | | |
|---|--------------------|-----------------|------------|---------------------------------|-----------------|----------|
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| | | | | Size | Document Number | Rev |
| | | | | Custom | LA-9201P | 0.1 |
| Date: | | | | Thursday, August 16, 2012 | Sheet | 43 of 66 |

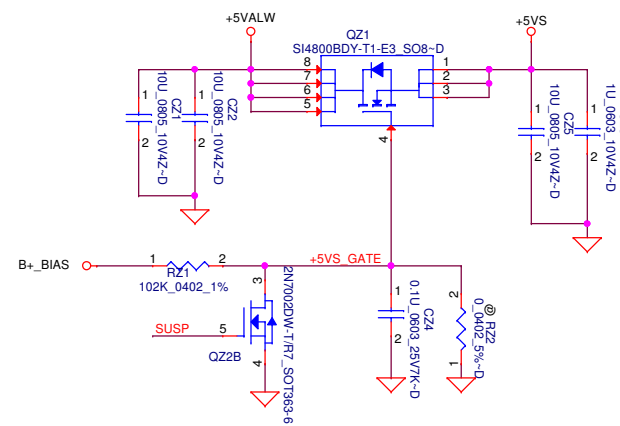


ZZZ1
PCB-MB

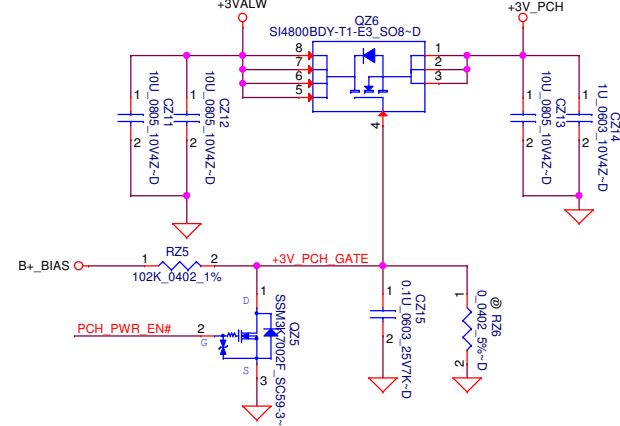
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|---|--------------------|-----------------|------------|------------------------|-----------------------------|
| Security Classification | Compal Secret Data | | | Title | |
| Issued Date | 2012/05/14 | Deciphered Date | 2013/05/13 | KB & Power Button & IR | |
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| | | | | Date: | Thursday, August 16, 2012 |
| | | | | Sheet | 44 of 66 |

DC to DC

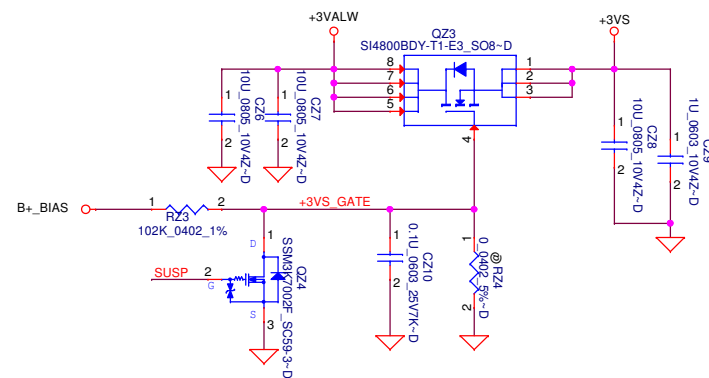
+5VALW to +5VS



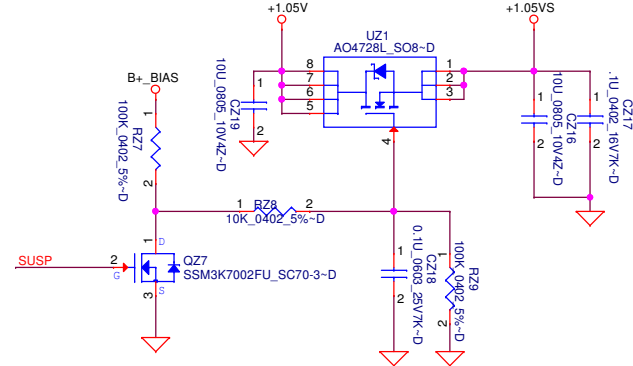
+3VALW to +3V_PCH



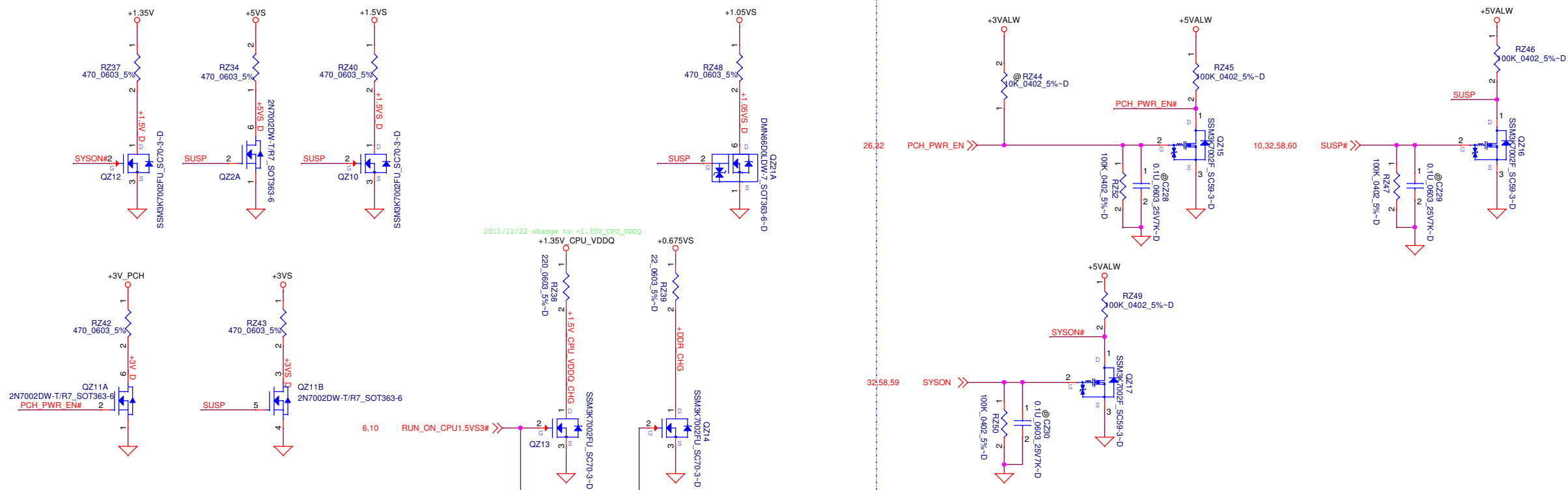
+3VALW to +3VS



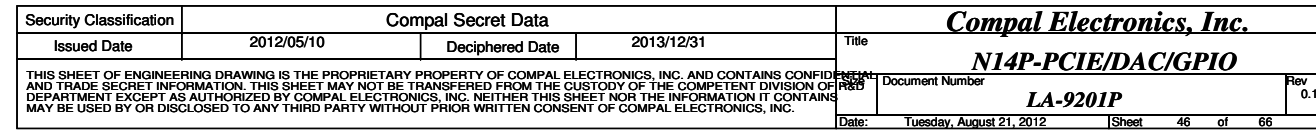
+1.05V To +1.05VS

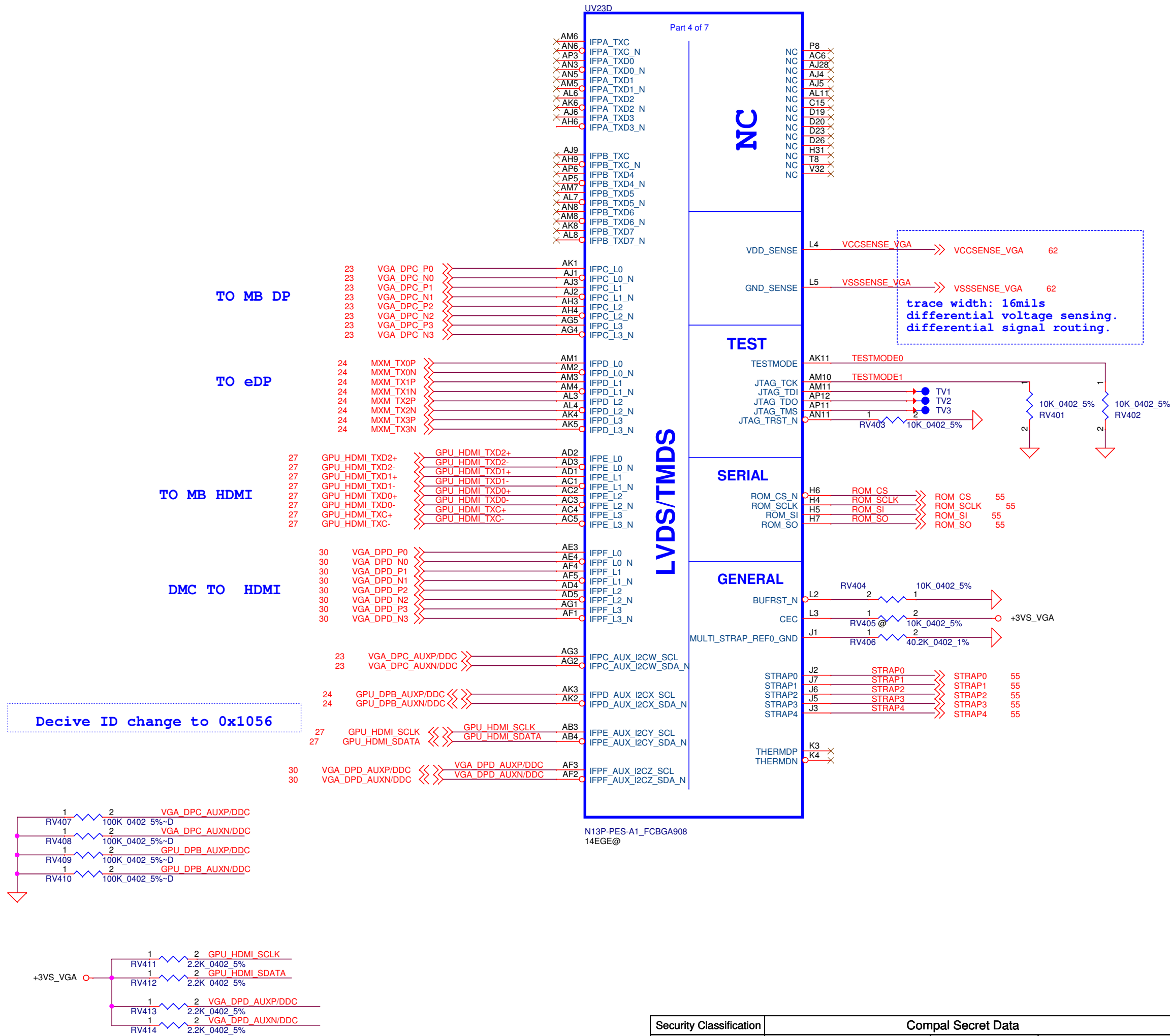


Discharge Circuit



| | | | | | | |
|---|------------|--------------------|------------|---|---------------------------|----------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. DC/DC Interface | | |
| Issued Date | 2012/05/14 | Deciphered Date | 2013/05/13 | Title | | |
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| | | | | Custom | LA-9201P | 0.1 |
| | | | | Date: | Thursday, August 16, 2012 | Sheet 45 of 66 |





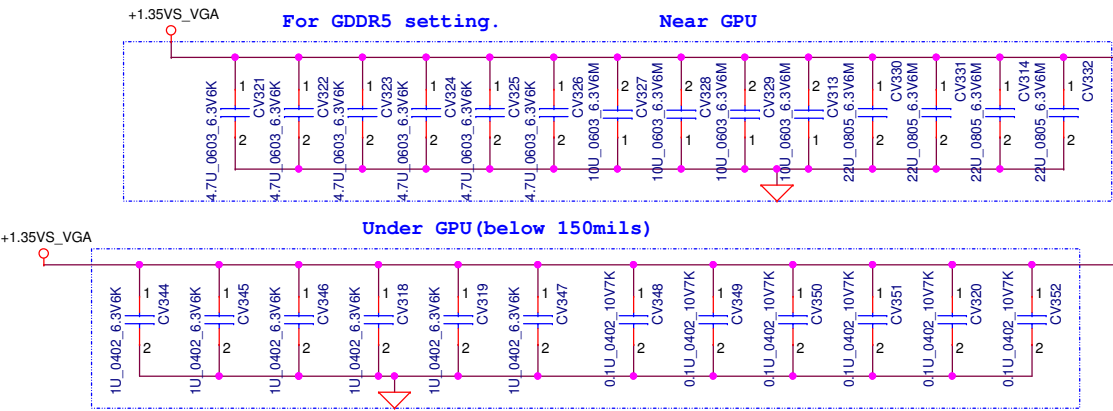
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| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | | 2012/05/10 | | Deciphered Date | |
| 2013/12/31 | | Document Number | | Rev | |
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| Tuesday, August 21, 2012 | | 1 | | 47 of 66 | |

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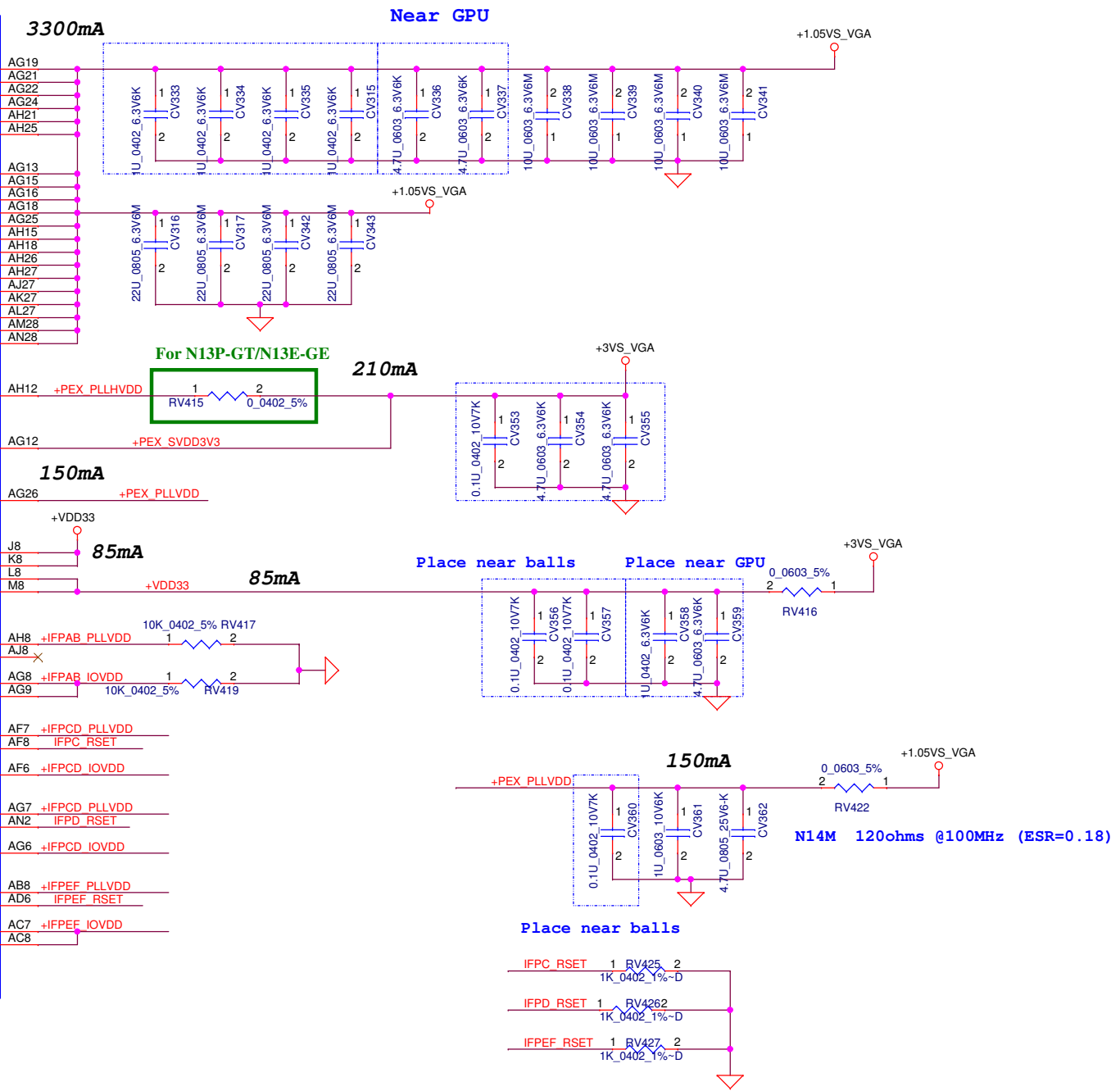
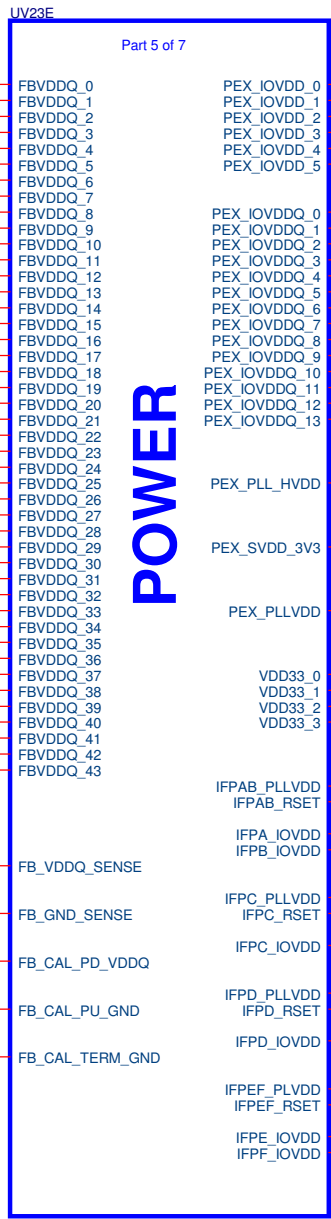
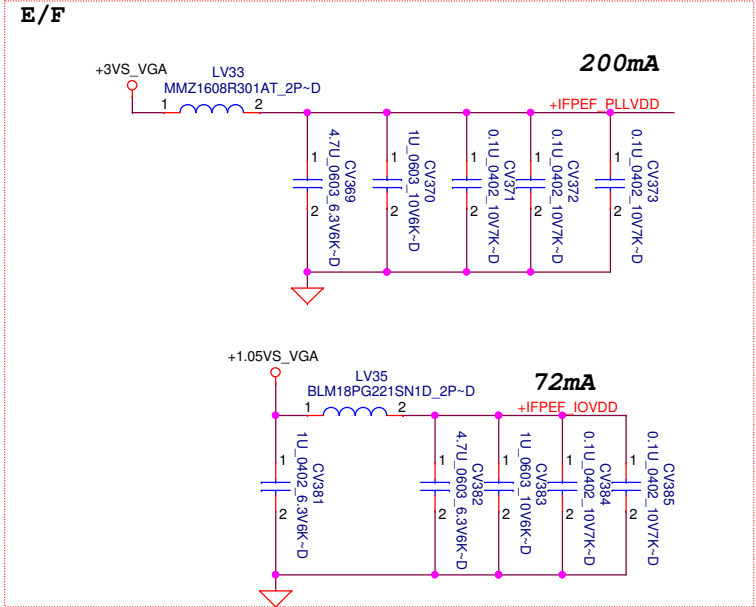
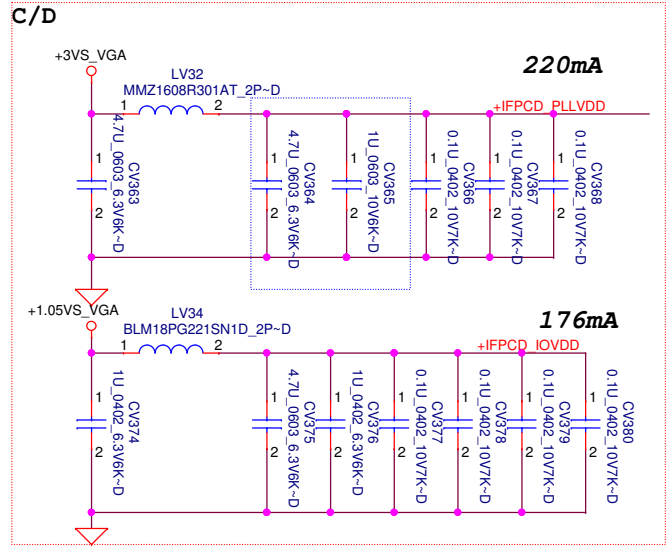
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LA-9201P

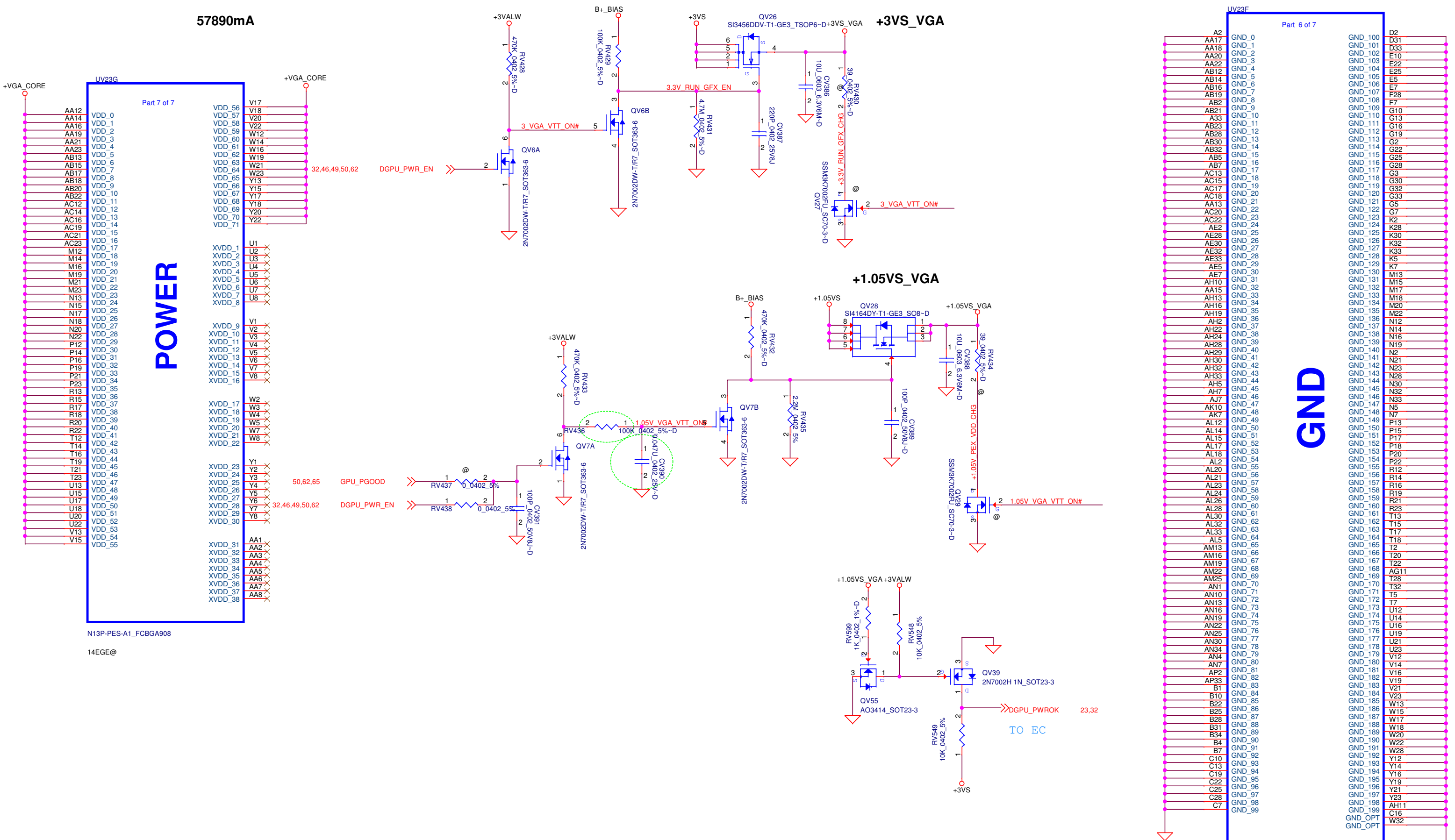
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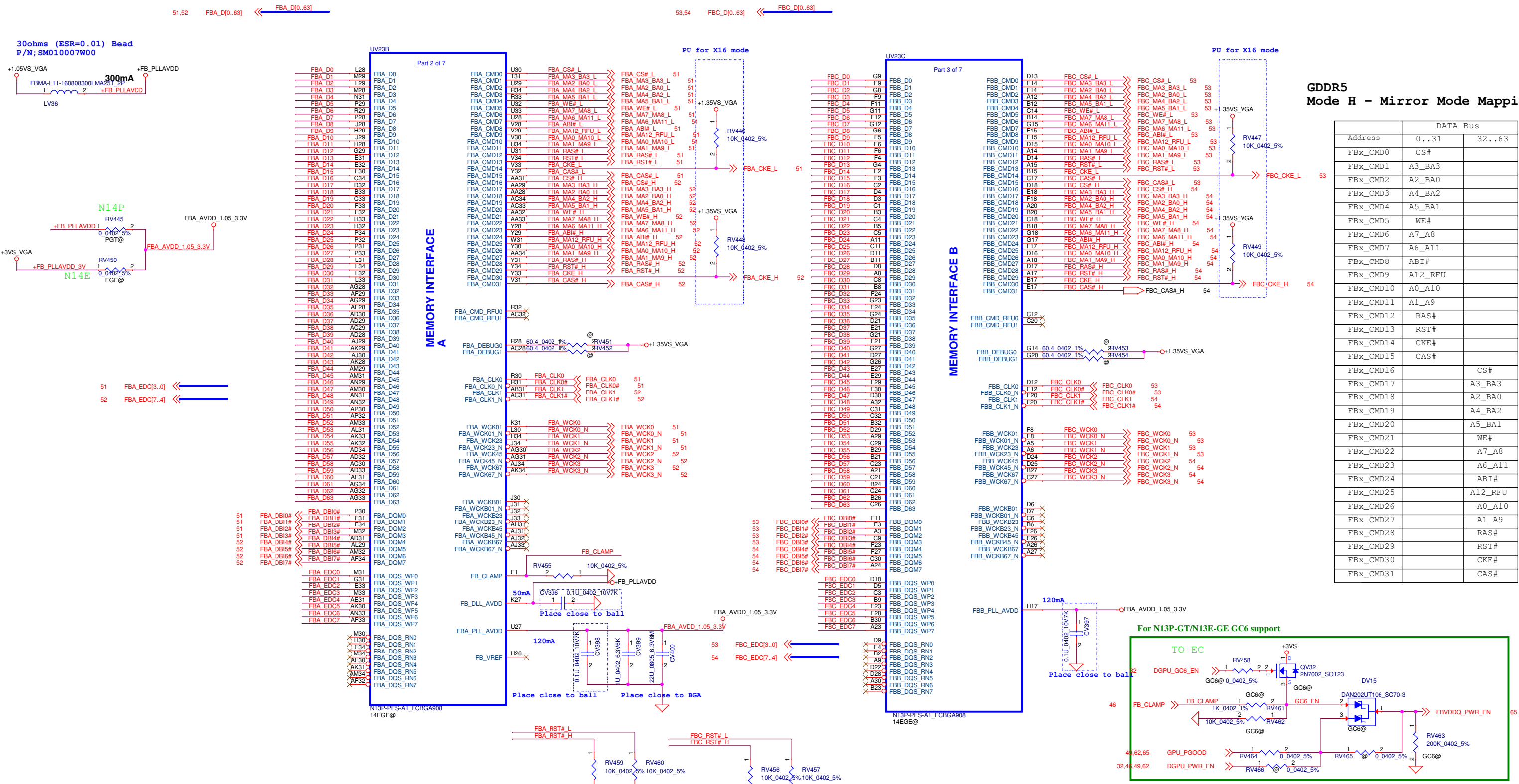
| | |
|------------------|---------|
| CALIBRATION PIN | GDDR5 |
| FB_CAL_x_PD_VDDQ | 40.2Ohm |
| FB_CAL_x_PU_GND | 40.2Ohm |
| FB_CAL_xTERM_GND | 60.4Ohm |



| | | | | | |
|---|------------|--------------------|------------|------------|--------------------------|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | 2012/05/10 | Deciphered Date | 2013/12/31 | N14P-POWER | |
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| | | | | LA-9201P | |
| | | | | Rev | 0.1 |
| | | | | Date: | Tuesday, August 14, 2012 |
| | | | | Sheet | 48 of 66 |



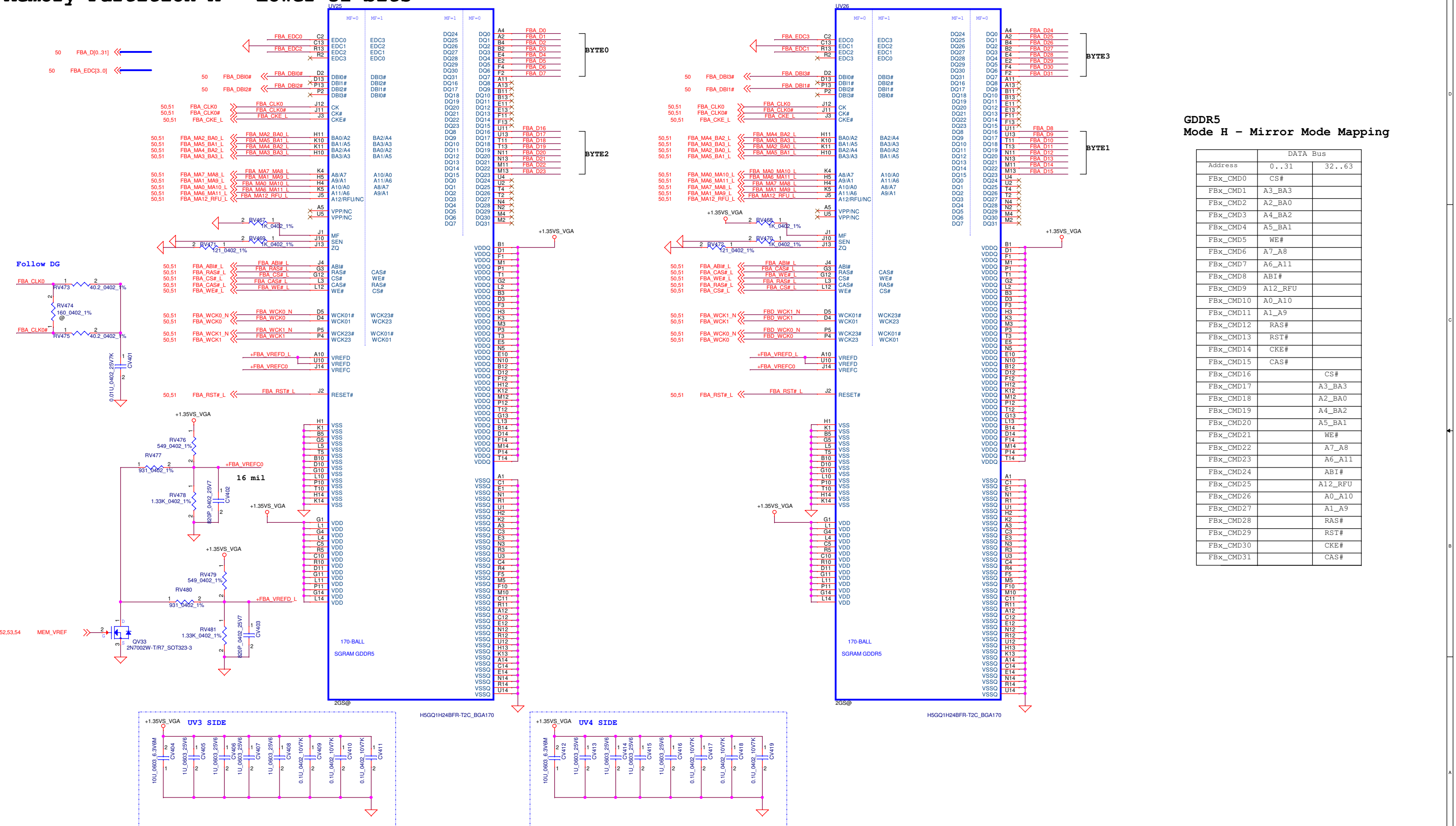
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|---|--------------------------|--------------------|------------|----------------------|--------------------------|
| Security Classification | | Compal Secret Data | | N13P-PES-A1_FCBGA908 | |
| Issued Date | 2012/05/10 | Deciphered Date | 2013/12/31 | Title | 14EGE@N14P-VGA CORE, GND |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. | | | | | |
| Size | Document Number | LA-9201P | | Rev | 0.1 |
| Date: | Tuesday, August 14, 2012 | Sheet | 49 | of | 66 |



GDDR5
Mode H - Mirror Mode Mapping

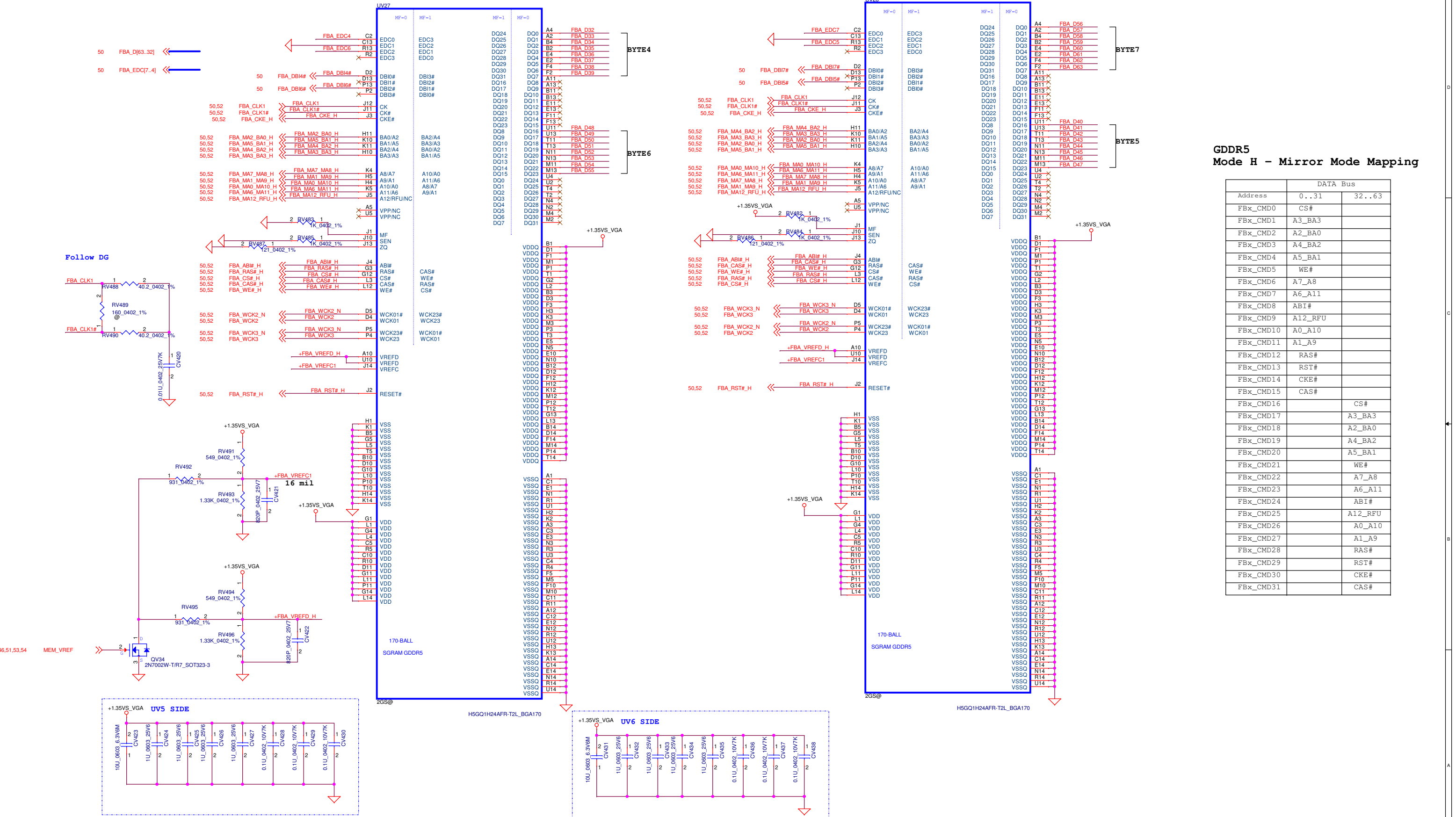
| DATA Bus | |
|-----------|--------------|
| Address | 0..31 32..63 |
| FBx_CMD0 | CS# |
| FBx_CMD1 | A3_BA3 |
| FBx_CMD2 | A2_BA0 |
| FBx_CMD3 | A4_BA2 |
| FBx_CMD4 | A5_BA1 |
| FBx_CMD5 | WE# |
| FBx_CMD6 | A7_A8 |
| FBx_CMD7 | A6_A11 |
| FBx_CMD8 | ABI# |
| FBx_CMD9 | A12_RFU |
| FBx_CMD10 | A0_A10 |
| FBx_CMD11 | A1_A9 |
| FBx_CMD12 | RAS# |
| FBx_CMD13 | RST# |
| FBx_CMD14 | CKE# |
| FBx_CMD15 | CAS# |
| FBx_CMD16 | |
| FBx_CMD17 | CS# |
| FBx_CMD18 | A3_BA3 |
| FBx_CMD19 | A2_BA0 |
| FBx_CMD20 | A4_BA2 |
| FBx_CMD21 | A5_BA1 |
| FBx_CMD22 | WE# |
| FBx_CMD23 | A7_A8 |
| FBx_CMD24 | A6_A11 |
| FBx_CMD25 | ABI# |
| FBx_CMD26 | A12_RFU |
| FBx_CMD27 | A0_A10 |
| FBx_CMD28 | A1_A9 |
| FBx_CMD29 | RAS# |
| FBx_CMD30 | RST# |
| FBx_CMD31 | CKE# |
| FBx_CMD32 | CAS# |

Memory Partition A - Lower 32 bits

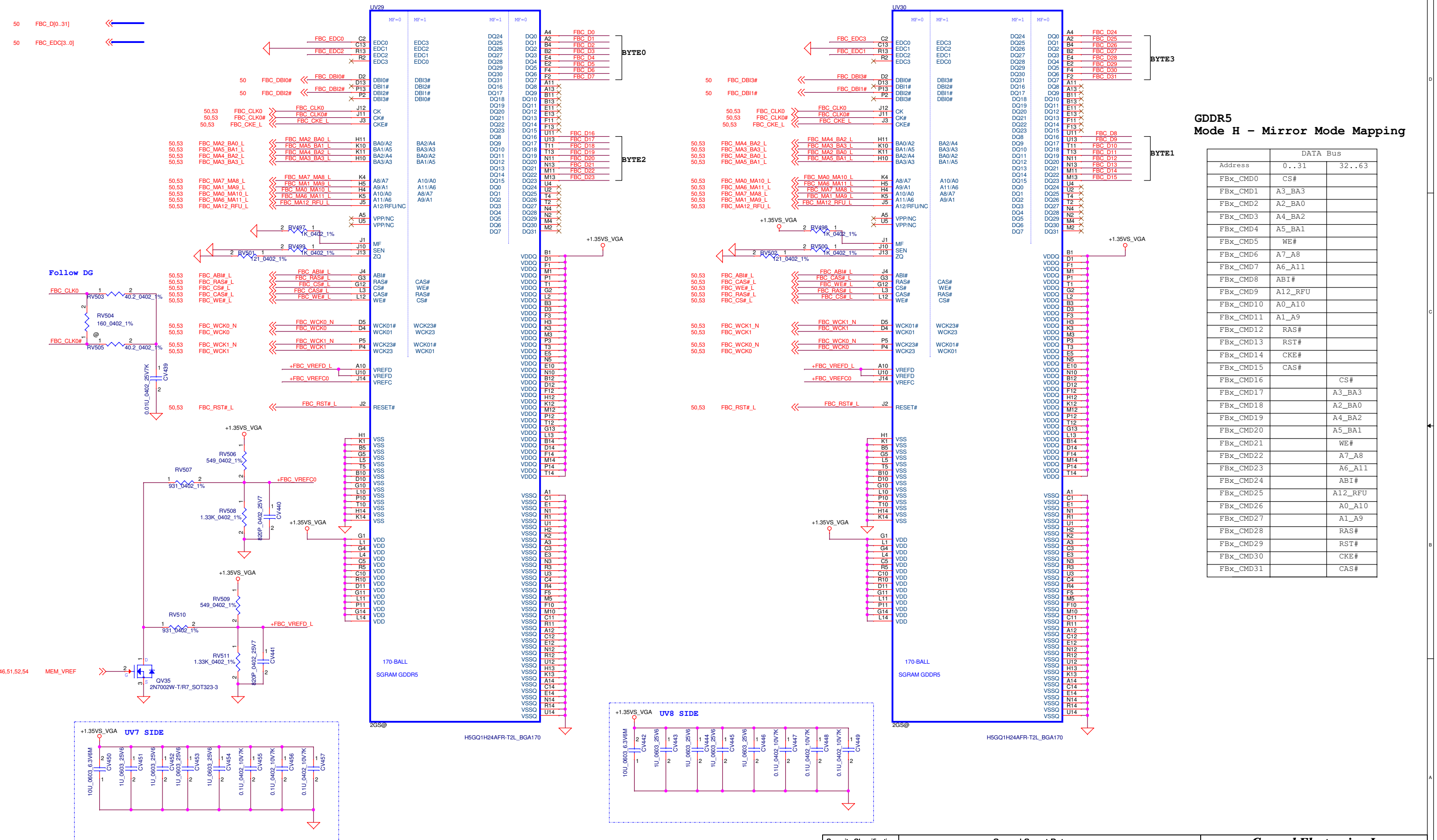


| GDDR5 | | |
|------------------------------|----------|---------|
| Mode H - Mirror Mode Mapping | | |
| Address | DATA Bus | |
| | 0..31 | 32..63 |
| FBx_CMD0 | CS# | |
| FBx_CMD1 | A3_BA3 | |
| FBx_CMD2 | A2_BA0 | |
| FBx_CMD3 | A4_BA2 | |
| FBx_CMD4 | A5_BA1 | |
| FBx_CMD5 | WE# | |
| FBx_CMD6 | A7_A8 | |
| FBx_CMD7 | A6_A11 | |
| FBx_CMD8 | ABI# | |
| FBx_CMD9 | A12_RFU | |
| FBx_CMD10 | A0_A10 | |
| FBx_CMD11 | A1_A9 | |
| FBx_CMD12 | RAS# | |
| FBx_CMD13 | RST# | |
| FBx_CMD14 | CKE# | |
| FBx_CMD15 | CAS# | |
| FBx_CMD16 | | CS# |
| FBx_CMD17 | | A3_BA3 |
| FBx_CMD18 | | A2_BA0 |
| FBx_CMD19 | | A4_BA2 |
| FBx_CMD20 | | A5_BA1 |
| FBx_CMD21 | | WE# |
| FBx_CMD22 | | A7_A8 |
| FBx_CMD23 | | A6_A11 |
| FBx_CMD24 | | ABI# |
| FBx_CMD25 | | A12_RFU |
| FBx_CMD26 | | A0_A10 |
| FBx_CMD27 | | A1_A9 |
| FBx_CMD28 | | RAS# |
| FBx_CMD29 | | RST# |
| FBx_CMD30 | | CKE# |
| FBx_CMD31 | | CAS# |

Memory Partition A - Upper 32 bits



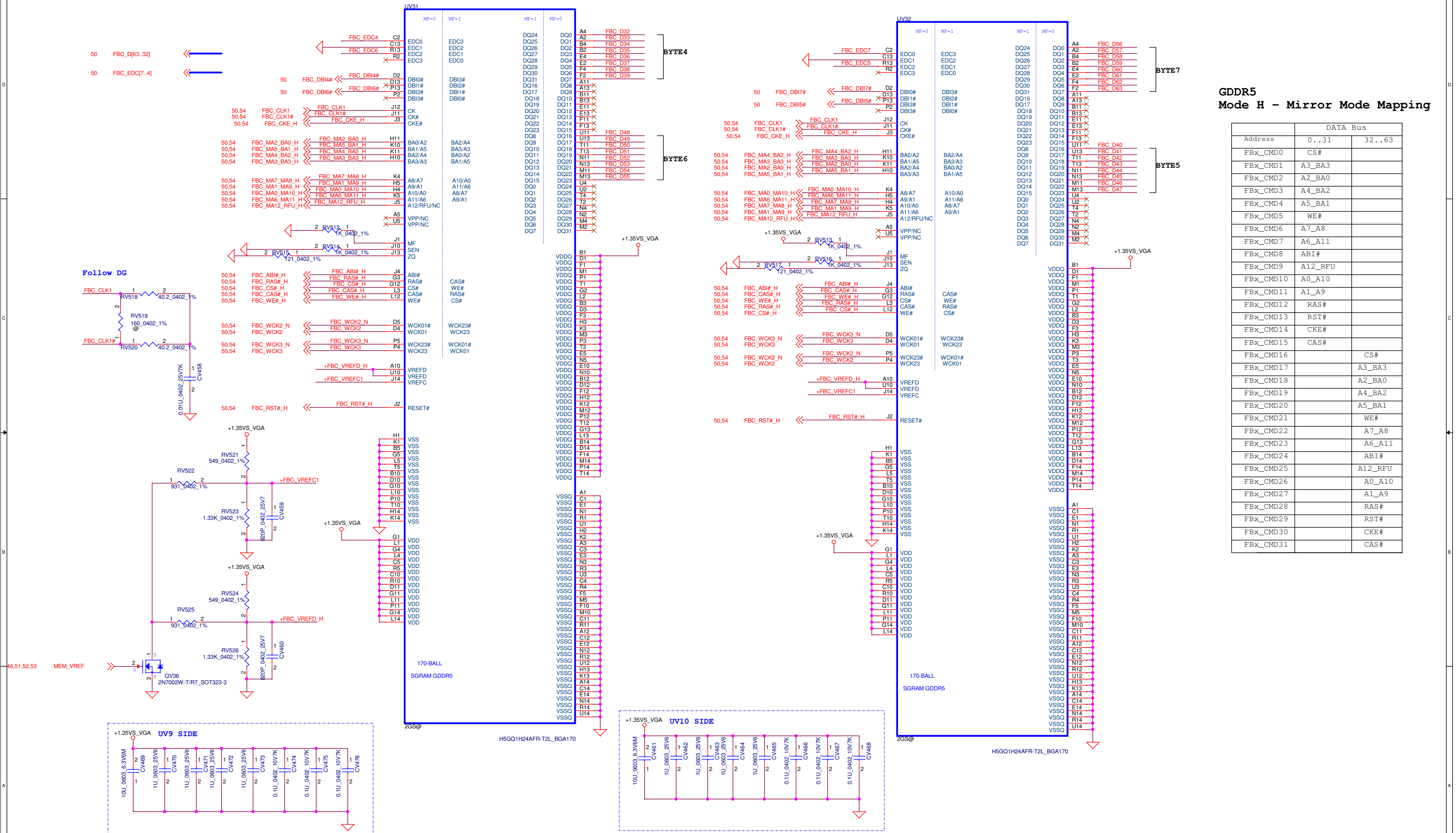
Memory Partition C - Lower 32 bits



GDDR5 Mode H - Mirror Mode Mapping

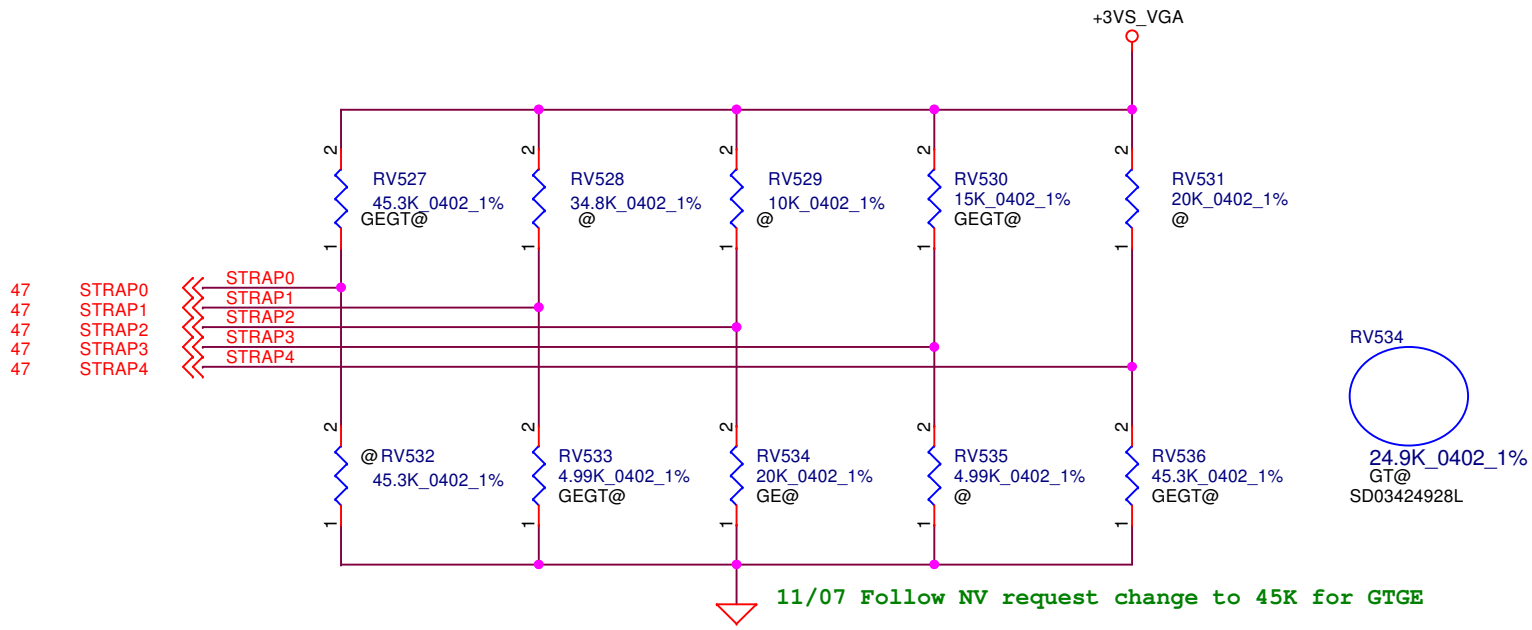
| Address | DATA Bus | |
|-----------|----------|---------|
| | 0..31 | 32..63 |
| FBx_CMD0 | CS# | |
| FBx_CMD1 | A3_BA3 | |
| FBx_CMD2 | A2_BA0 | |
| FBx_CMD3 | A4_BA2 | |
| FBx_CMD4 | A5_BA1 | |
| FBx_CMD5 | WE# | |
| FBx_CMD6 | A7_A8 | |
| FBx_CMD7 | A6_A11 | |
| FBx_CMD8 | ABI# | |
| FBx_CMD9 | A12_RFU | |
| FBx_CMD10 | A0_A10 | |
| FBx_CMD11 | A1_A9 | |
| FBx_CMD12 | RAS# | |
| FBx_CMD13 | RST# | |
| FBx_CMD14 | CKE# | |
| FBx_CMD15 | CAS# | |
| FBx_CMD16 | | CS# |
| FBx_CMD17 | | A3_BA3 |
| FBx_CMD18 | | A2_BA0 |
| FBx_CMD19 | | A4_BA2 |
| FBx_CMD20 | | A5_BA1 |
| FBx_CMD21 | | WE# |
| FBx_CMD22 | | A7_A8 |
| FBx_CMD23 | | A6_A11 |
| FBx_CMD24 | | ABI# |
| FBx_CMD25 | | A12_RFU |
| FBx_CMD26 | | A0_A10 |
| FBx_CMD27 | | A1_A9 |
| FBx_CMD28 | | RAS# |
| FBx_CMD29 | | RST# |
| FBx_CMD30 | | CKE# |
| FBx_CMD31 | | CAS# |

Memory Partition C - Upper 32 bits

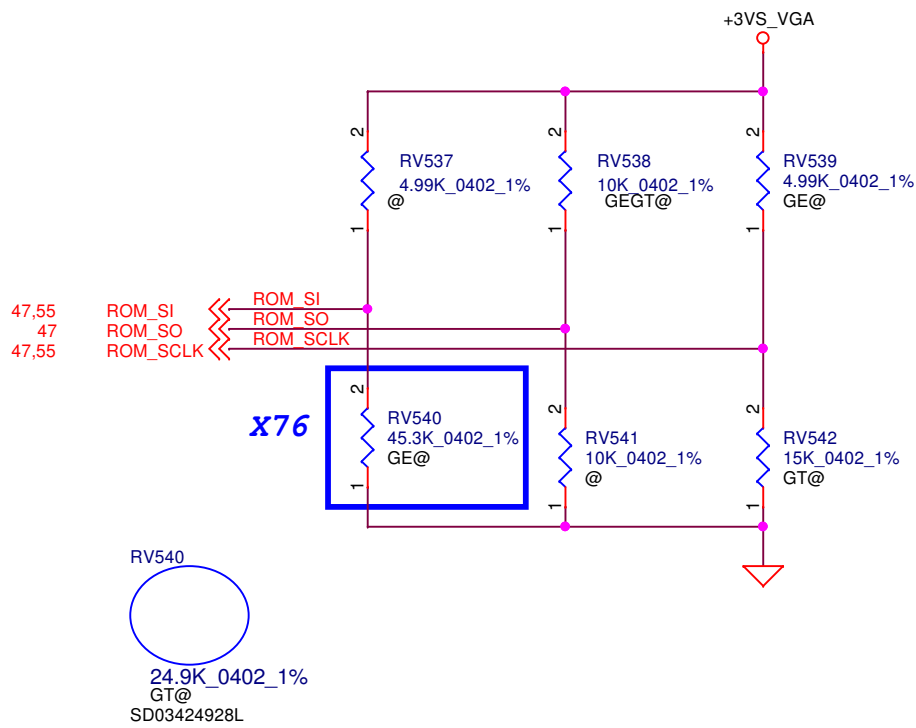


GDDR5 Mode H - Mirror Mode Mapping

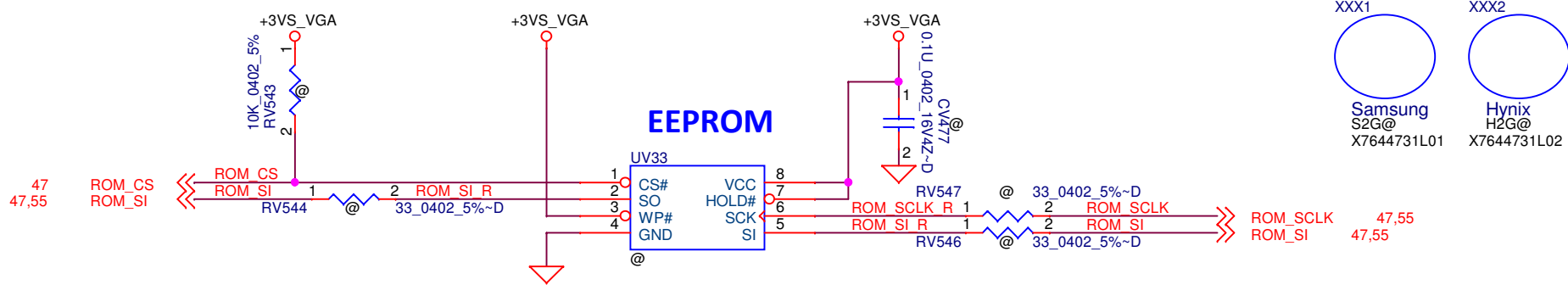
| Address | DATA Bus | |
|-----------|----------|---------|
| | 0..31 | 32..63 |
| FBx_CMD0 | CS# | |
| FBx_CMD1 | A3_BA3 | |
| FBx_CMD2 | A2_BA0 | |
| FBx_CMD3 | A4_BA2 | |
| FBx_CMD4 | A5_BA1 | |
| FBx_CMD5 | WE# | |
| FBx_CMD6 | A7_A8 | |
| FBx_CMD7 | A6_A11 | |
| FBx_CMD8 | ABI# | |
| FBx_CMD9 | A12_RFU | |
| FBx_CMD10 | A0_A10 | |
| FBx_CMD11 | A1_A9 | |
| FBx_CMD12 | RAS# | |
| FBx_CMD13 | RST# | |
| FBx_CMD14 | CKE# | |
| FBx_CMD15 | CAS# | |
| FBx_CMD16 | | CS# |
| FBx_CMD17 | | A3_BA3 |
| FBx_CMD18 | | A2_BA0 |
| FBx_CMD19 | | A4_BA2 |
| FBx_CMD20 | | A5_BA1 |
| FBx_CMD21 | | WE# |
| FBx_CMD22 | | A7_A8 |
| FBx_CMD23 | | A6_A11 |
| FBx_CMD24 | | ABI# |
| FBx_CMD25 | | A12_RFU |
| FBx_CMD26 | | A0_A10 |
| FBx_CMD27 | | A1_A9 |
| FBx_CMD28 | | RAS# |
| FBx_CMD29 | | RST# |
| FBx_CMD30 | | CKE# |
| FBx_CMD31 | | CAS# |



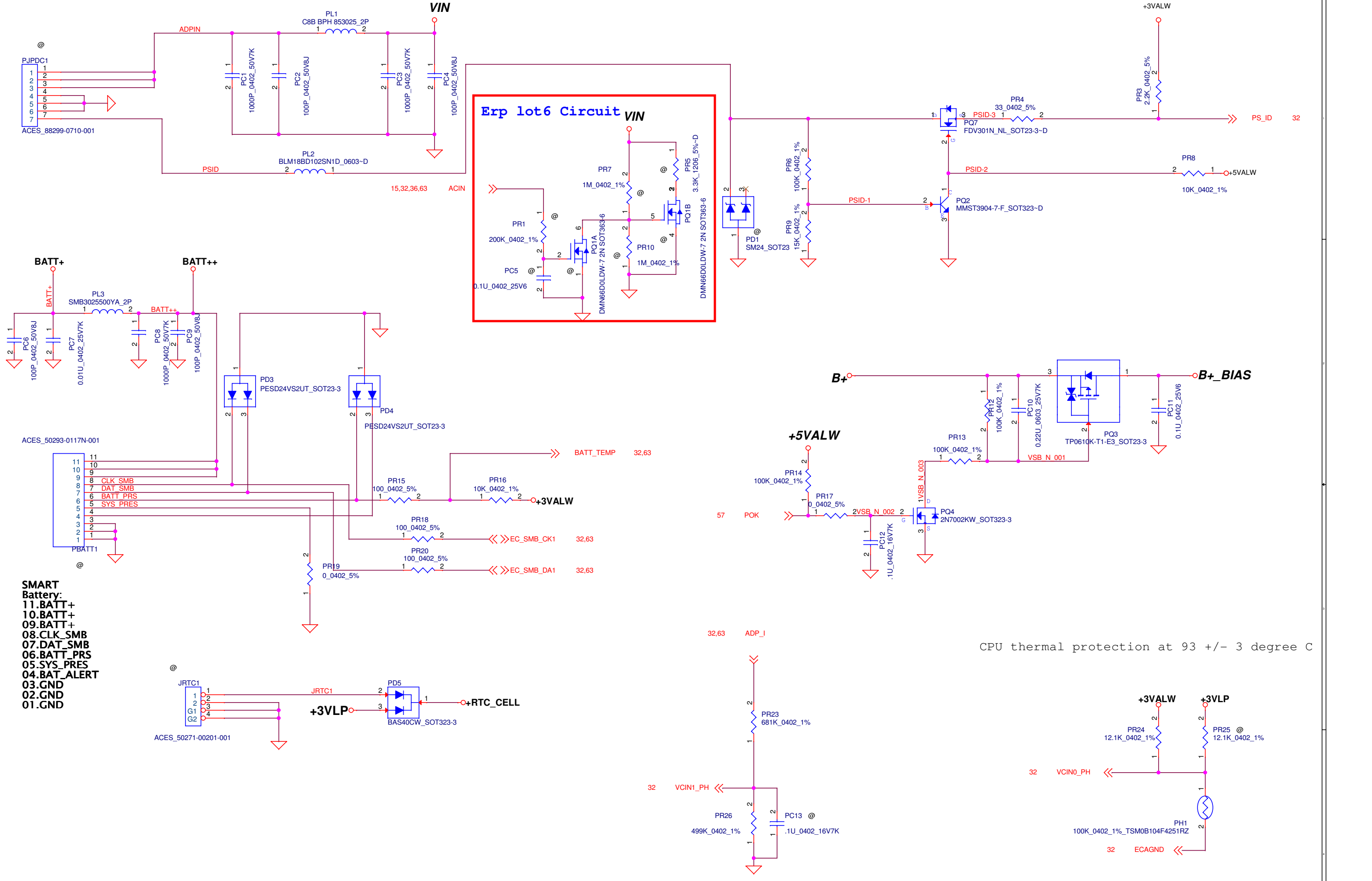
N14E-GE (ver.ES) SA00005W30L Samsung SA00005B70L
N14P-GT (ver.ES) SA00005W20L Hynix SA00004GD1L



| GPU | FB Memory gDDR5 | ROM_SO | ROM_SCLK | ROM_SI | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---------|-----------------|-----------------|---------------|--------|--------|--------|--------|--------|--------|
| N14P-GT | Samsung 900MHz | | | | | | | | |
| | 128Mx16 | | | | | | | | |
| | Hynix 900MHz | H5GQ2H24AER-T2C | PU 10K PD 15K | PD 25K | PU 45K | PD 5K | PD 25K | PU 15K | PD 45K |
| | 128Mx16 | | | | | | | | |
| N14E-GE | Samsung 900MHz | K4G20325FD-FC04 | PU 10K PU 5K | PD 45K | PU 45K | PD 5K | PD 20K | PU 15K | PD 45K |
| | 128Mx16 | | | | | | | | |
| | Hynix 900MHz | | | | | | | | |
| | 128Mx16 | | | | | | | | |



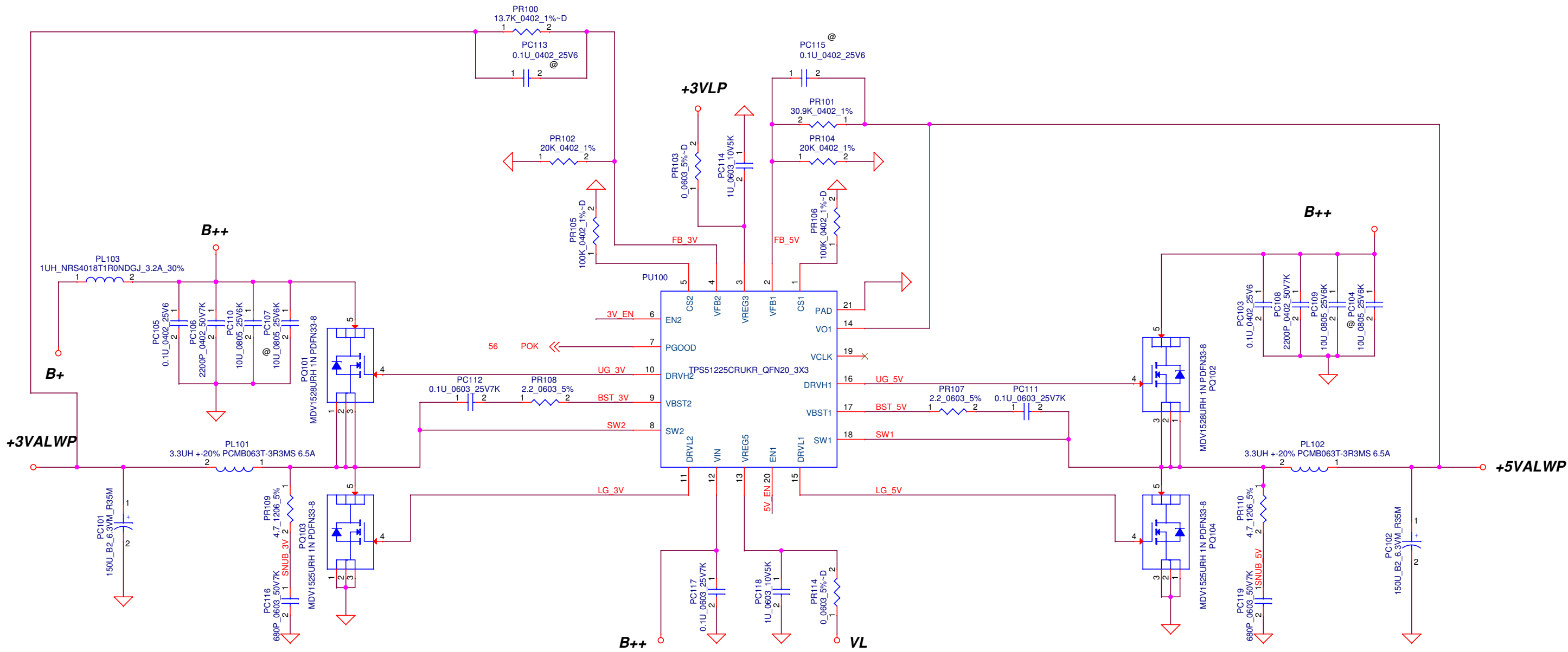
| | | | | | |
|---|--------------------|-----------------|------------|-------------------------------|----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2012/05/10 | Deciphered Date | 2013/12/31 | Title | |
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| | | | | Size Custom | Rev 0.1 |
| | | | | Document Number | LA-9201P |
| | | | | Date: Friday, August 17, 2012 | Sheet 55 of 66 |



SMART
Battery:
11.BATT+
10.BATT+
09.BATT+
08.CLK_SMB
07.DAT_SMB
06.BATT_PRS
05.SYS_PRES
04.BAT_ALERT
03.GND
02.GND
01.GND

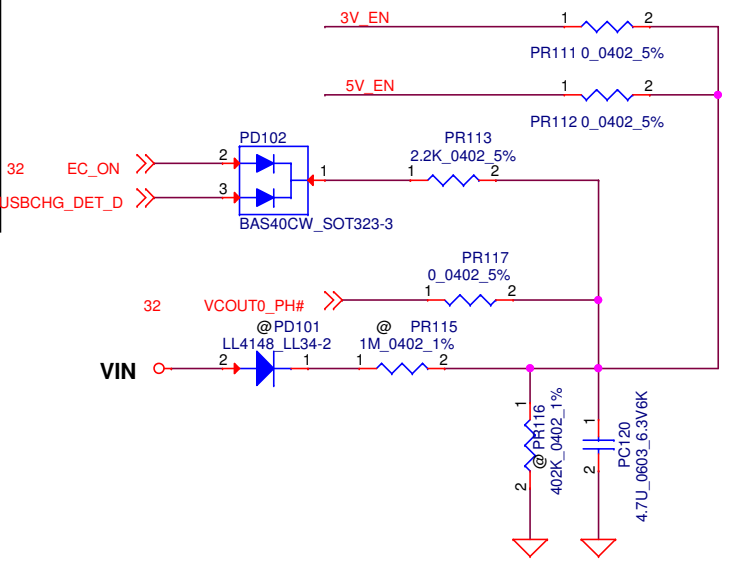
CPU thermal protection at 93 +/- 3 degree C

| | | | | | |
|---|------------|--------------------|------------|--------------------------|----------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 | Title | PWR-DCIN / BATT CONN / OTP |
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| | | | | Rev | 0.1 |
| Date: Friday, August 10, 2012 | | Sheet 56 | | of 66 | |

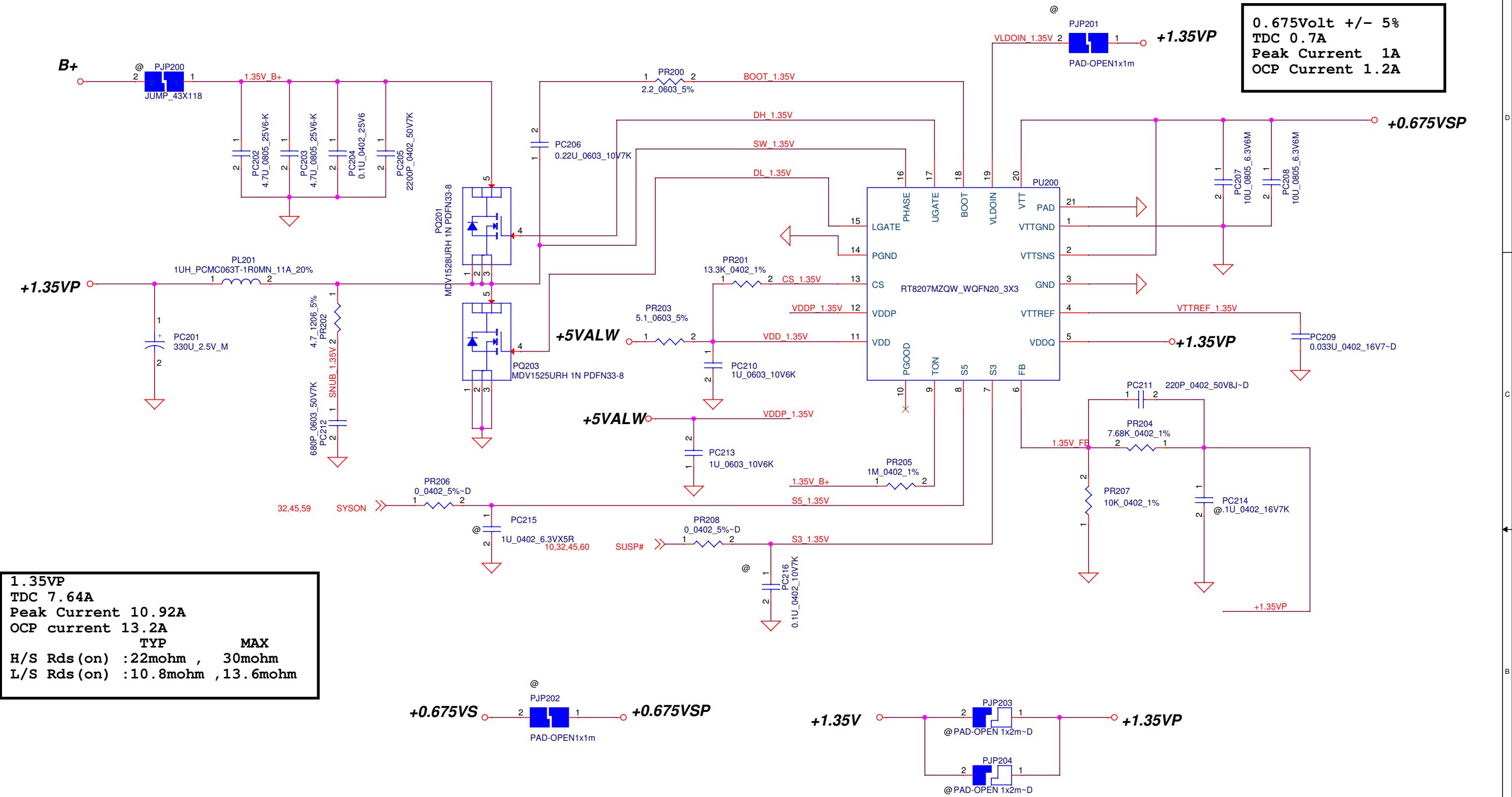


3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A
TYP MAX
H/S Rds (on) : 22mohm , 30mohm
L/S Rds (on) : 10.8mohm , 13.6mohm

5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A
TYP MAX
H/S Rds (on) : 22mohm , 30mohm
L/S Rds (on) : 10.8mohm , 13.6mohm



| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|-------------------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 | Title | PWR-3VALWP/5VALWP |
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| | | | | Rev | 0.1 |
| | | | | Date: | Friday, August 10, 2012 |
| | | | | Sheet | 57 of 66 |

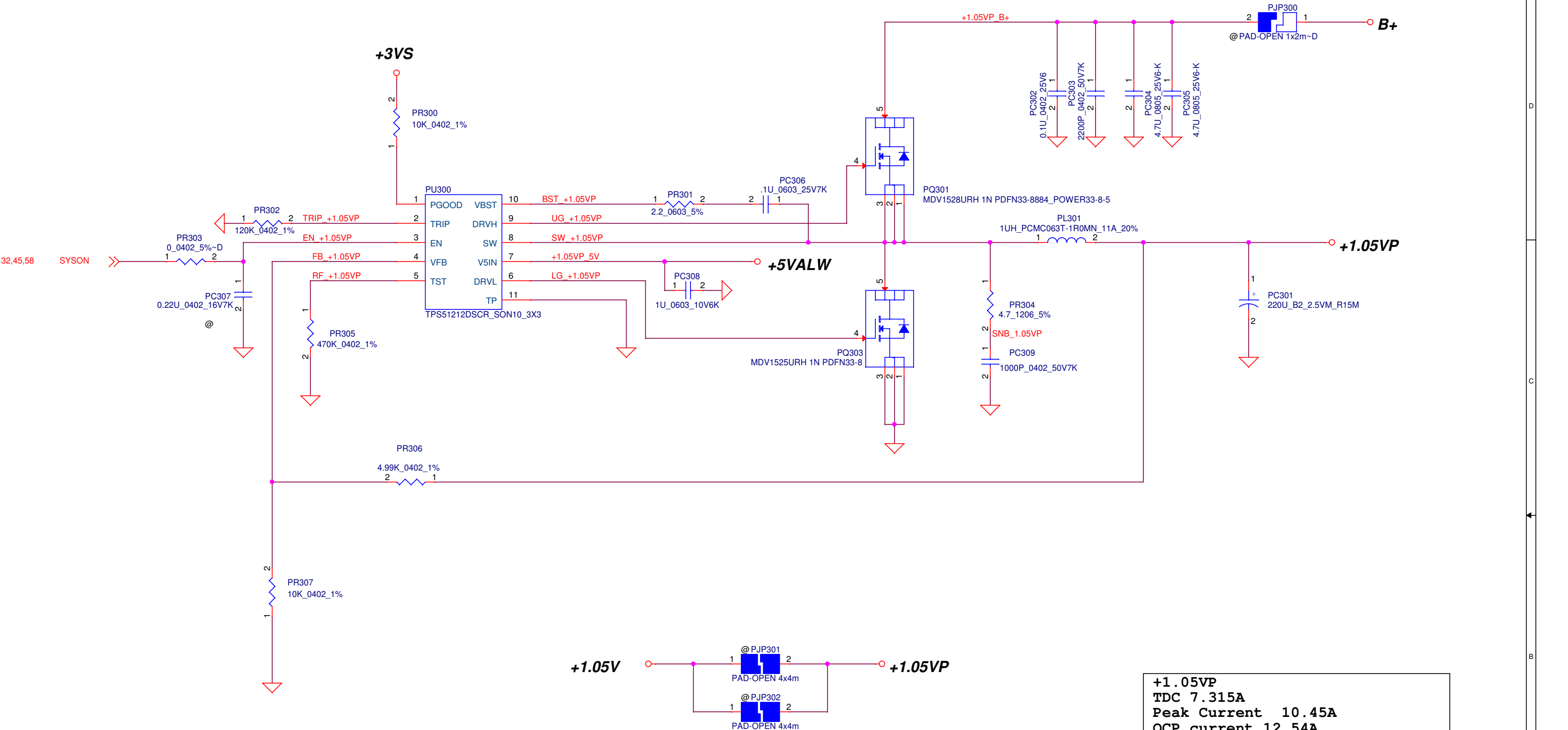


1.35VP
TDC 7.64A
Peak Current 10.92A
OCP current 13.2A

| | TYP | MAX |
|--------------|-----------|------------|
| H/S Rds (on) | :22mohm | , 30mohm |
| L/S Rds (on) | :10.8mohm | , 13.6mohm |

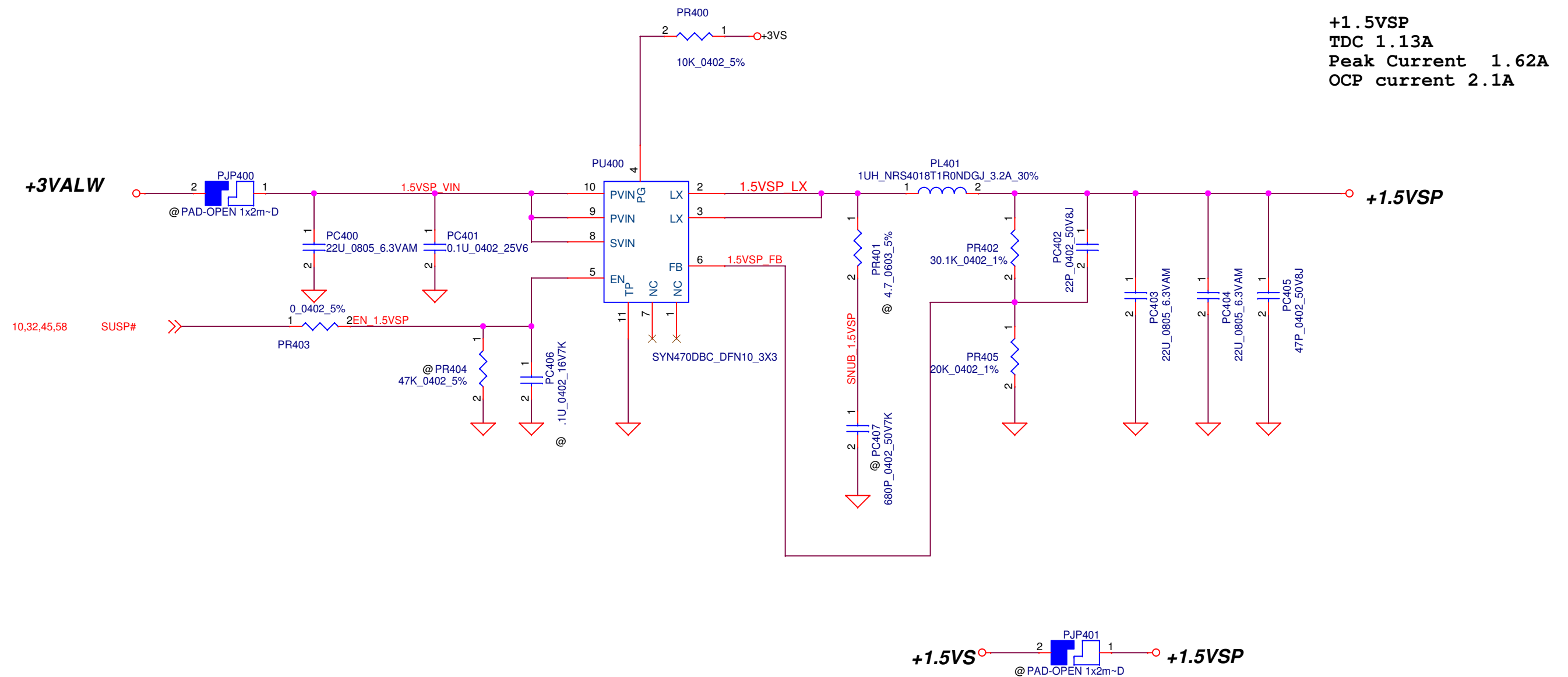
0.675Vlt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

| | | | | | |
|---|------------|-------------------------|------------|--------------------------|-----------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 | Title | |
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| | | | | | LA-XXXXP |
| | | | | Rev | 0.1 |
| Date: | | Friday, August 10, 2012 | | Sheet | 58 of 66 |



| | |
|--------------|----------------------|
| +1.05VP | |
| TDC 7.315A | |
| Peak Current | 10.45A |
| OCp current | 12.54A |
| TYP MAX | |
| H/S Rds (on) | :22mohm , 30mohm |
| L/S Rds (on) | :10.8mohm , 13.6mohm |

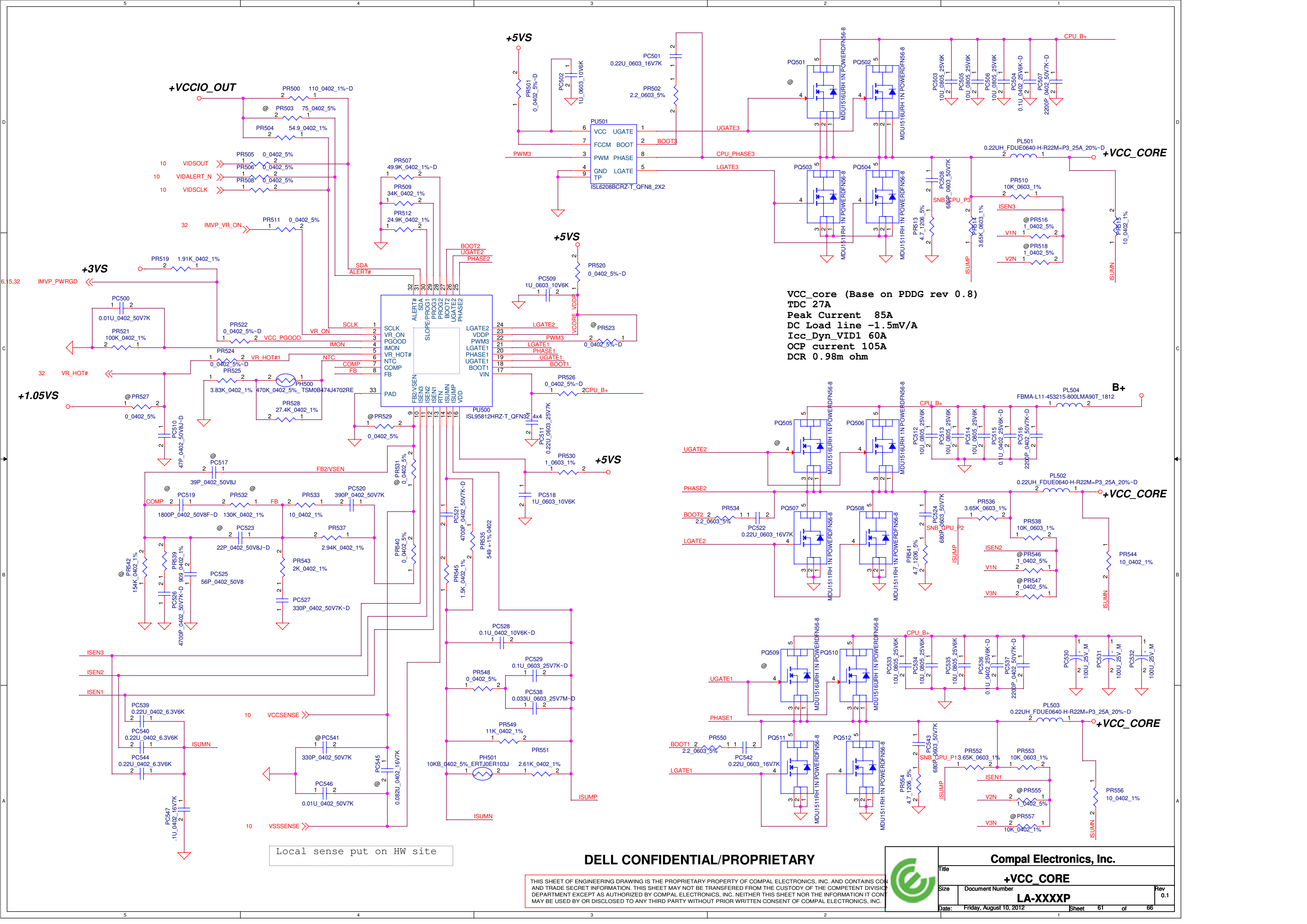
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 | Title | |
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| | | | | | LA-XXXXP |
| | | | | Rev | 0.1 |
| Date: | | Friday, August 10, 2012 | | Sheet | 59 of 66 |



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| | | | |
|--------------------------|-------------------------|------------|----------------|
| Compal Electronics, Inc. | | | |
| Title | | PWR-1.5VSP | |
| Size | Document Number | | Rev |
| | LA-7902P | | 0.1 |
| Date: | Friday, August 10, 2012 | | Sheet 60 of 66 |



+VCCIO_OUT

+3VS

+1.05VS

+5VS

+5VS

+5VS

CPU B+

+VCC_CORE

B+

+VCC_CORE

+VCC_CORE

Local sense put on HW site

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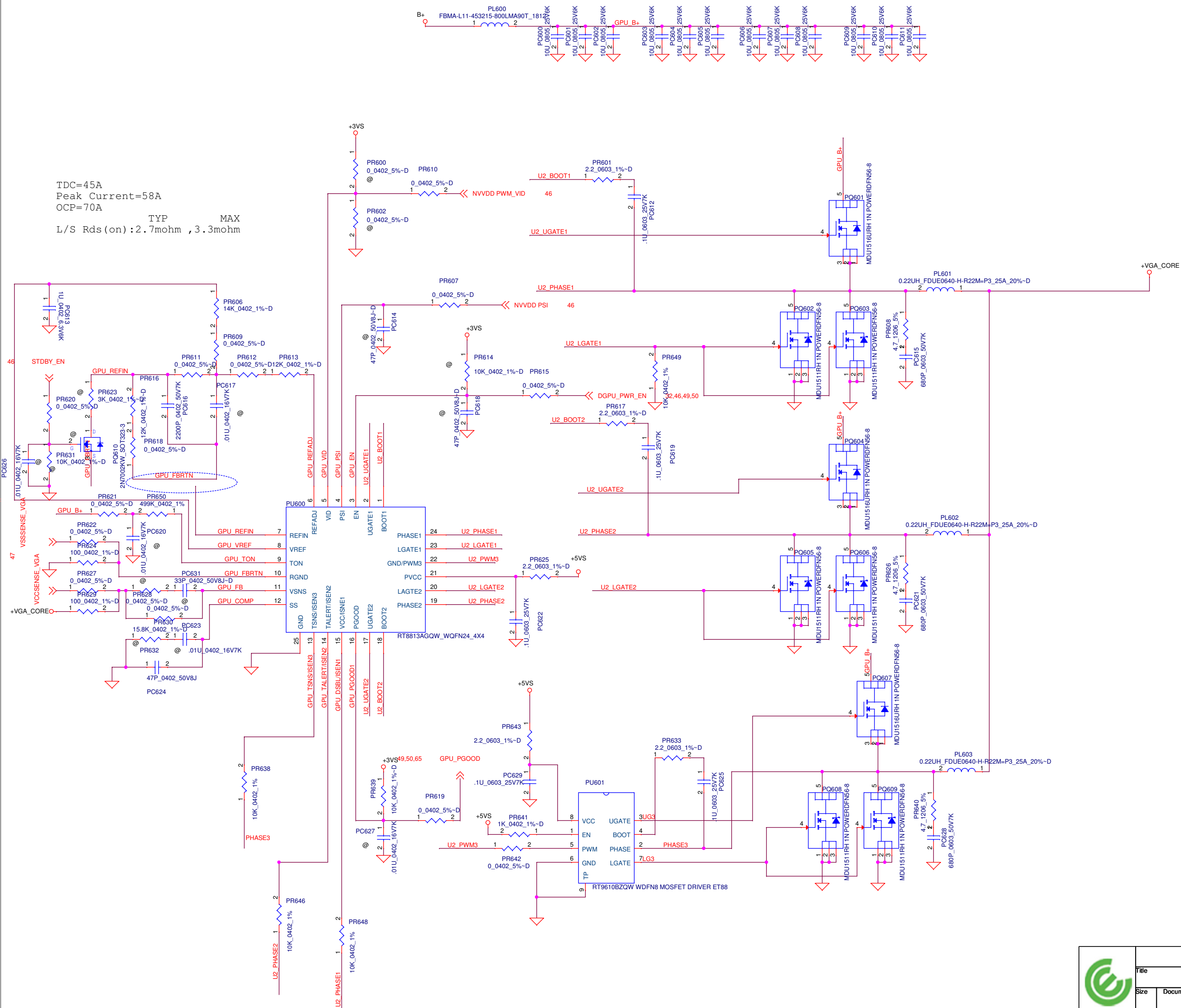
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| | | |
|--------------------------|-------------------------|----------------|
| Compal Electronics, Inc. | | |
| +VCC_CORE | | |
| Size | Document Number | Rev |
| | LA-XXXXP | 0.1 |
| Date: | Friday, August 10, 2012 | Sheet 61 of 66 |

TDC=45A
Peak Current=58A
OCP=70A

| | TYP | MAX |
|--------------|---------|---------|
| L/S Rds(on): | 2.7mohm | 3.3mohm |



Compal Electronics, Inc.

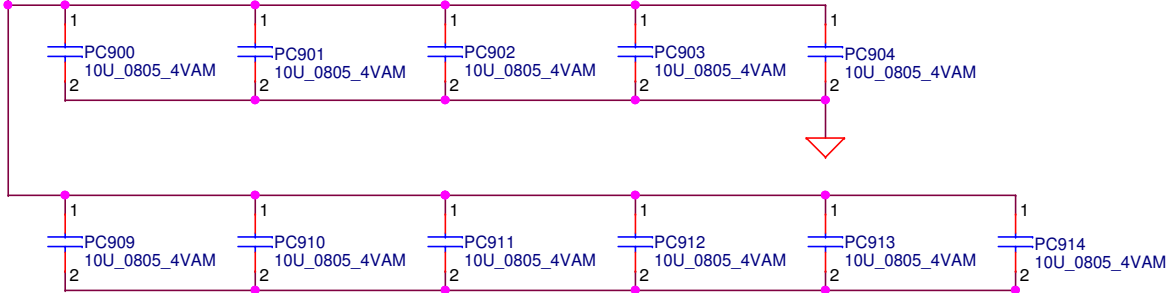
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| Title | +VGA_CORE |
|-------|------------------|

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|------|-----------------|
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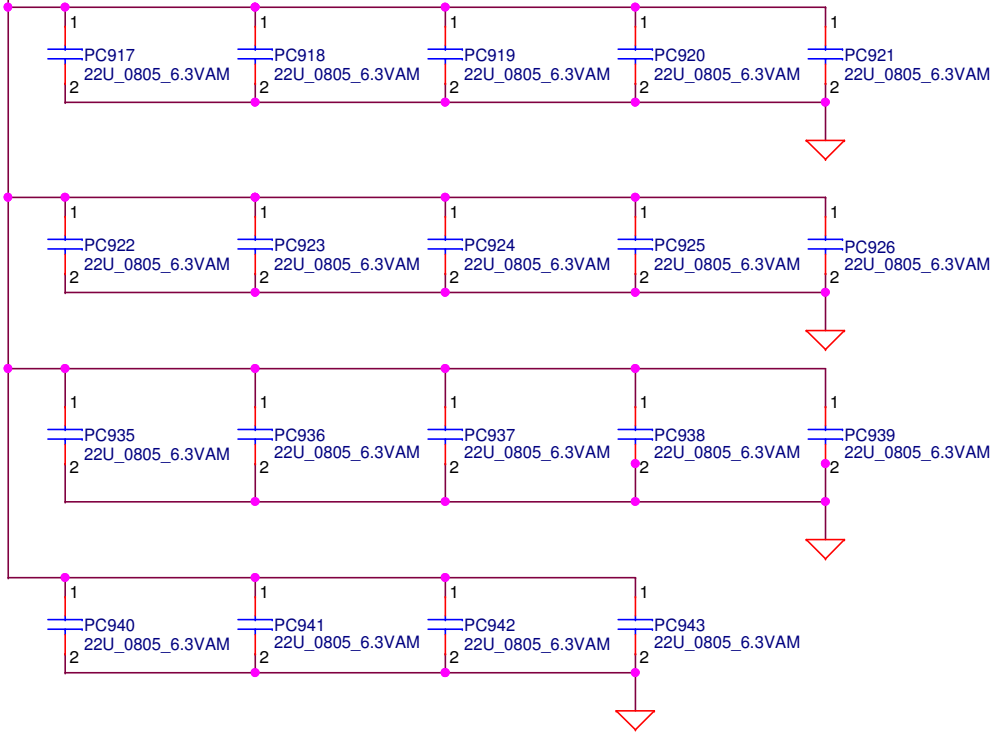
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|-----|-----|
| Rev | 0.1 |
|-----|-----|

Based on PDDG rev 0.7 Table 5-1.

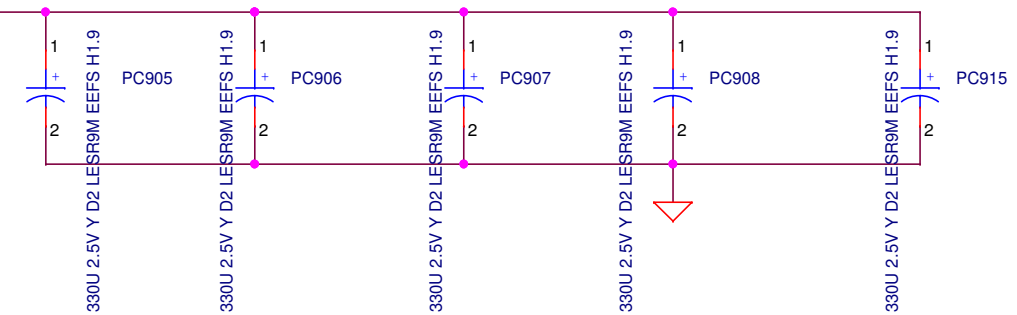
+VCC_CORE



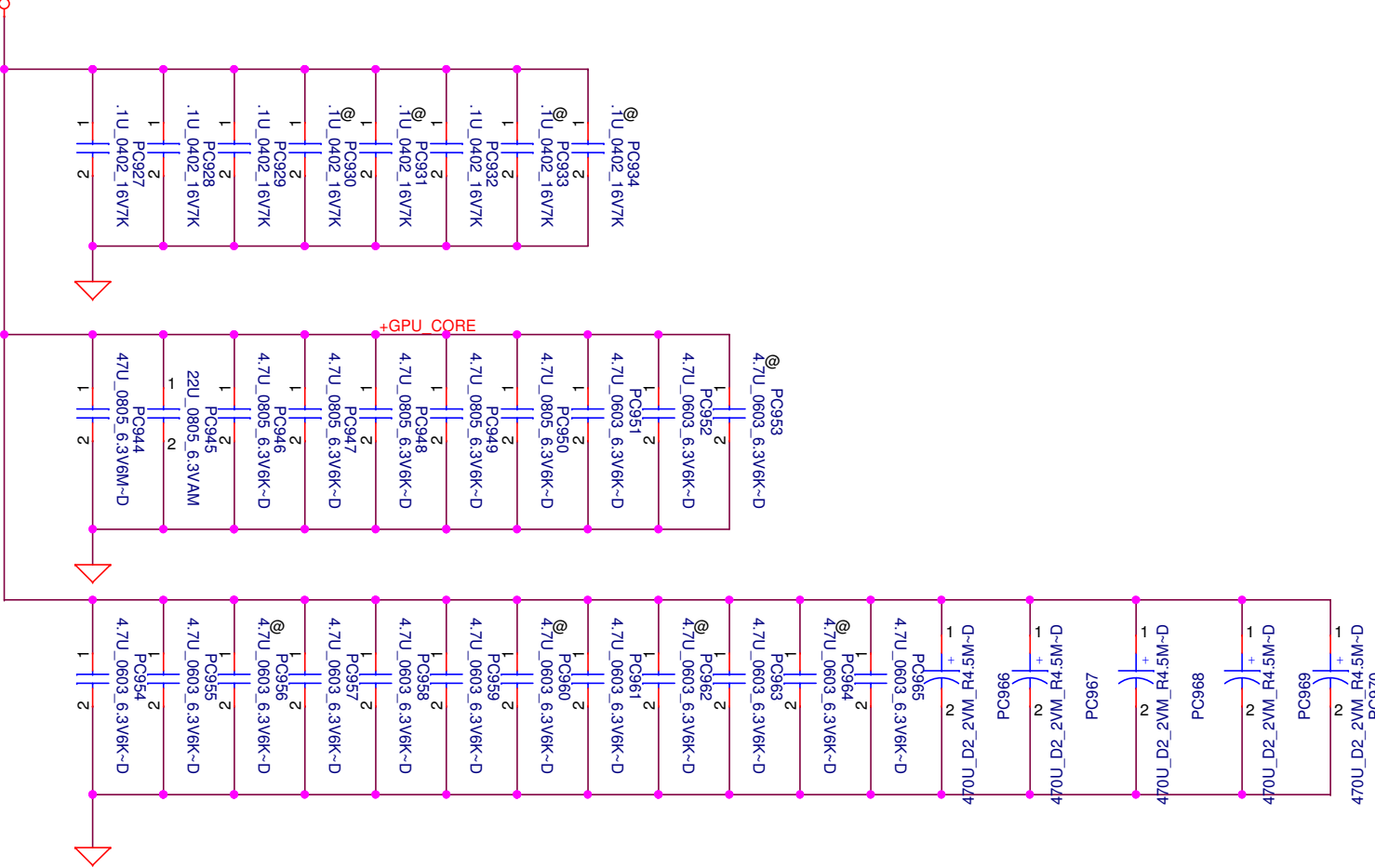
+VCC_CORE



+VCC_CORE



+VGA_CORE

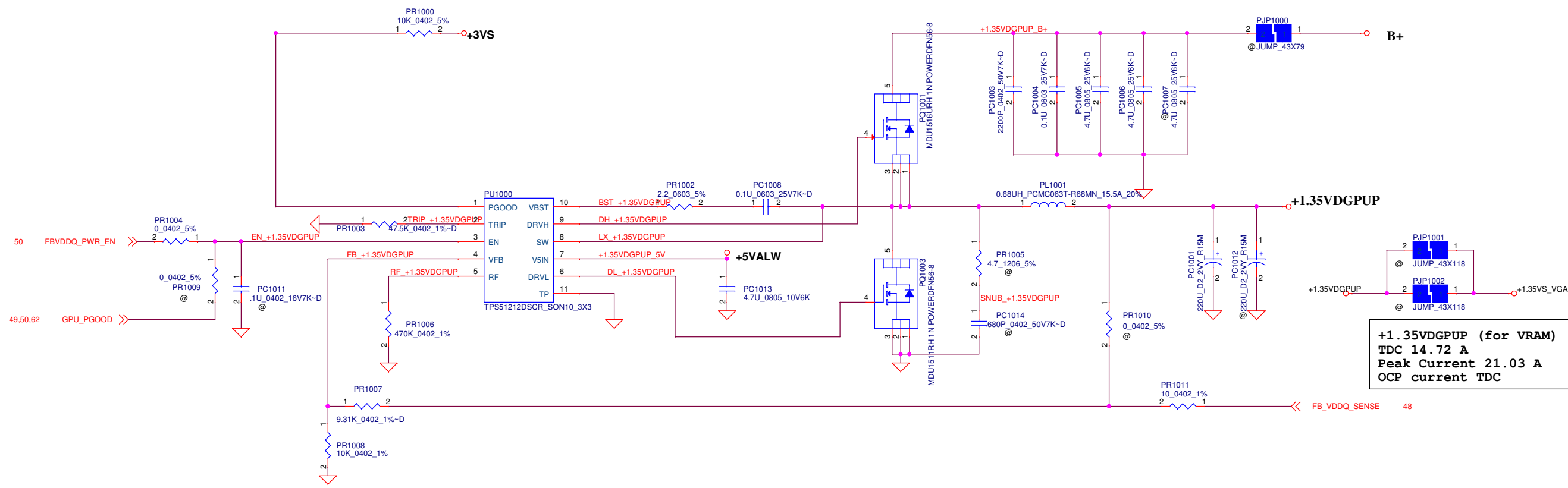


DELL CONFIDENTIAL/PROPRIETARY



| Compal Electronics, Inc. | | | |
|--------------------------|-------------------------|--|----------------|
| Title | | | |
| PROCESSOR DECOUPLING | | | |
| Size | Document Number | | Rev |
| | LA-XXXXP | | 0.1 |
| Date: | Friday, August 10, 2012 | | Sheet 64 of 66 |


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| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|------|----------|-------|------|---------------|--|---|------|
| 1 | 56 | Power | 7/24 | Compal | HW and Power has the same part | PD5 pin1 change from +RTC_BATT to +RTC_CELL | |
| 2 | 57 | Power | 7/24 | Compal | Shortage issue | PC111、PC112 change from SE042104M80 to SE042104K8L | |
| 3 | 56 63 | Power | 7/24 | Compal | Shortage issue | PQ1,PQ710,PQ716,PQ717,PQ718 change from SB000000600 to SB000000DH0L | |
| 4 | 56 | Power | 7/24 | Compal | Adapter protect function | PR23 change from 340K ohm to 681K ohm | |
| 5 | 56 | Power | 7/24 | Compal | For De-rating | PR530 change size from 0402 to 0603 | |
| 6 | 57 | Power | 7/30 | Compal | For OTP | Del PD100.Add PR117 | |
| 7 | 64 | Power | 7/30 | Compal | Update Memo | Change SGA0000420L to SGA0000268L PC905,PC906,PC907,PC908,PC915 | |
| 8 | 62 | Power | 7/30 | Compal | For VGA CORE | Change PU600 from UP1642 to RT8831A Change PU601 from UP1909 to RT9610B | |
| 9 | 62 | Power | 8/1 | Compal | For VGA CORE | Change PR638,PR646,PR648 from 2k to 10k Unpop PR632,PC623 Add PC624 47pF Unpop PR628,PC631 Add PR630,PR620 o ohm Change PR650 from 68.1k to 499k Change PC616 from 0.01uF to 2.2nF Add PR649 10k ohm | |
| 10 | 58 | Power | 8/3 | Compal | For 1.35V output voltage and Dfx request | Change PR204 from 8.06k to 7.65k Change PJP203,PJP204 size from 4x4m to 1x2m | |
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| Size | Document Number LA-9201P | | Rev 0.2 |
| Date: Friday, August 10, 2012 | | Sheet 66 | of 66 |